MG0307A
OPERATIONS MANUAL

M-W0949AE-1.0

MG0307A

π/4 DQPSK Modulation Unit

Operation Manual
(Panel Operating Instructions)

(Blank)

CERTIFICATION

ANRITSU CORPORATION certifies that this instrument has been thoroughly tested and inspected, and found to meet published specifications prior to shipping.
Anritsu further certifies that its calibration measurements are based on the Japanese Electrotechnical Laboratory and Radio Research Laboratory standards.

WARRANTY

All parts of this product are warranted by Anritsu Corporation of Japan against defects in material or workmanship for a period of one year from the date of delivery.
In the event of a defect occurring during the warranty period, Anritsu Corporation will repair or replace this product within a reasonable period of time after notification, free-of-charge, provided that: it is returned to Anritsu; has not been misused; has not been damaged by an act of God; and that the user has followed the instructions in the operation manual.

Any unauthorized modification, repair, or attempt to repair, will render this warranty void.

This warranty is effective only for the original purchaser of this product and is not transferable if it is resold.

ALL OTHER EXPRESSED WARRANTIES ARE DISCLAIMED AND ALL IMPLIED WARRANTIES FOR THIS PRODUCT, INCLUDING THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE LIMITED IN DURATION TO A PERIOD OF ONE YEAR FROM THE DATE OF DELIVERY. IN NO EVENT SHALL ANRITSU CORPORATION BE LIABLE TO THE CUSTOMER FOR ANY DAMAGES, INCLUDING LOST PROFITS, OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES, ARISING OUT OF THE USE OR INABILITY TO USE THIS PRODUCT.

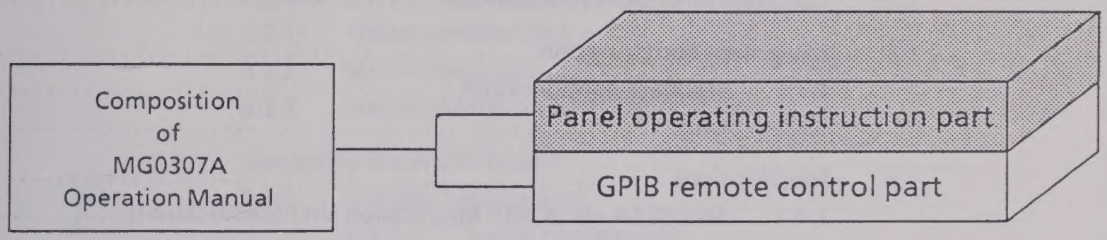
All requests for repair or replacement under this warranty must be made as soon as possible after the defect has been noticed and must be directed to Anritsu Corporation or its representative in your area.

(Blank)

ABOUT THIS MANUAL

(1) Composition of MG0307A Operation Manuals

The operation manual of the MG0307A (π/4 DQPSK Modulation Unit) is composed of the following two parts. The related operations of the MG0303B (Burst Function Unit) are also explained.



Panel Operating Instructions part: Provides information on the MG0307A outline, preparation before use, manual (local) operation, measuremant, performance test, storage, transportation, screen transition, communication system, and error message.

GPIB remote control part: Provides information on the MG0307A remote control which conforms with IEEE488.2 standards. To assist creating GPIB programs, this part gives examples of N88 BASIC language programs that run on the NEC Corp. PC9800 series of personal computers.

(2) The relations between the installed units and the expanded functions

The MG0307A (π/4 DQPSK Modulation Unit) and the MG0303B (Burst Function Unit) are expansion units, and are inserted in the MG3670 series Digital Modulation Signal Generator. The relations between the installed units and the expanded functions are explained below:

Units installed	Modulation system	Modulation pattern	RF output
MG0307A only	π/4 DQPSK Modulation • Bit rate: 384 kbps, Filter: $\alpha = 0.5$ • Bit rate: 1152kbps, Filter: $\alpha = 0.5$	• PN9/PN15-stage pseudorandom pattern • Free 4/16-bit repetition pattern	• Continuous wave
MG0307A + MG0303B	π/4 DQPSK Modulation • Bit rate: 384 kbps, Filter: $\alpha = 0.5$ • Bit rate: 1152kbps, Filter: $\alpha = 0.5$	• PN9/PN15-stage pseudorandom pattern • Free 4/16-bit repetition pattern • Pattern conforming to the systems	• Continuous wave • Burst wave

TABLE OF CONTENTS

SECTION 1 GENERAL 1-1

1.1 Product Outline 1-3

1.2 Composition of Operation Manual 1-4

1.3 Equipment Configuration 1-5
1.3.1 Standard configuration 1-5
1.3.2 Unit 1-5

1.4 Specifications 1-6
1.4.1 MG0307A π/4 DQPSK Modulation Unit specifications 1-6
1.4.2 MG0303B Burst Function Unit specifications 1-7

SECTION 2 BASIC OPERATION 2-1

2.1 Screen Transition 2-3

2.2 Setting the Modulation Parameters 2-4

2.3 Setting Internal Modulation Data 2-7

2.4 Internal Modulation Data Memory 2-9
2.4.1 Saving internal modulation data 2-9
2.4.2 Recalling internal modulation data 2-13
2.4.3 Deleting internal modulation data 2-14
2.4.4 Listing internal modulation data 2-16

2.5 I, Q Signal Outputs 2-17

2.6 Auxiliary signal outputs 2-19
2.6.1 Data, data clock and symbol clock signals 2-19
2.6.2 Pattern sync signal 2-19
2.6.3 Burst gate signal 2-22

2.7 Auxiliary Inputs Signal 2-24
2.7.1 Data, data clock and symbol clock signals 2-24
2.7.2 Burst gate signal 2-24

2.8 Symbol Adjust Function 2-25

2.9 Phase Encode Function 2-26

SECTION 3 DETAILED OPERATIONS 3-1

3.1 Operating the PACS System 3-3
3.1.1 Frame composition 3-3
3.1.2 Slot composition 3-3
3.1.3 Standard internal modulation data 3-5

3.2 Operating the PHS System 3-7
3.2.1 Frame composition 3-7
3.2.2 Slot composition 3-7
3.2.3 Standard internal modulation data 3-11

3.3 Operating the WCPE System 3-14
3.3.1 Full Slot transmission 3-14
3.3.1.1 Frame composition 3-14
3.3.1.2 Slot composition 3-14
3.3.1.3 Standard internal modulation data 3-17
3.3.2 Double Slot transmission 3-23
3.3.2.1 Frame composition 3-23
3.3.2.2 Slot composition 3-23
3.3.2.3 Standard internal modulation data 3-25
3.3.3 Half Slot transmission 3-28
3.3.3.1 Frame composition 3-28
3.3.3.2 Slot composition 3-28
3.3.3.3 Standard internal modulation data 3-30

3.4 Detailed Trigger Function 3-33
3.4.1 Operation of the internal trigger 3-33
3.4.2 Operation of the external trigger 3-33
3.4.3 Output Timing of Burst Trigger and RF Signals 3-35
3.4.4 Relationships Between RF Signal and Symbol Judgment Point 3-38

SECTION 4 MEASUREMENT 4-1

4.1 Code Error Rate Measurement for Receiver 4-3

4.2 Demodulator Evaluation Measurement 4-5

4.3 Modulator Evaluation Measurement 4-6

SECTION 5 PERFORMANCE TESTS 5-1

5.1 Performance Tests Requirement 5-3

5.2 Instruments Required for Performance Tests 5-3

5.3 Performance Tests 5-4

5.3.1 I/Q signal modulation accuracy 5-4

5.3.2 RF output modulation accuracy 5-6

5.3.3 Modulation pattern 5-7

5.3.4 Burst signal On/Off ratio 5-8

5.3.5 Leakage power of adjacent channel characteristics 5-10

SECTION 1
GENERAL

This section outlines the MG0307A π/4 DQPSK Modulation Unit and explains the composition of this manual, the configuration of the MG0307A the standard accessories, with the related unit for expanding the MG0307A capabilities, and the MG0303B specifications.

TABLE OF CONTENTS

1.1 Product Outline 1-3

1.2 Composition of Operation Manual 1-4

1.3 Equipment Configuration 1-5

1.3.1 Standard configuration 1-5

1.3.2 Unit 1-5

1.4 Specifications 1-6

1.4.1 MG0307A π / 4 DQPSK Modulation Unit specifications 1-6

1.4.2 MG0303B Burst Function Unit specifications 1-7

(Blank)

SECTION 1
GENERAL

1.1 Product Outline

The MG0307A $\pi/4$ DQPSK Modulation Unit and the MG0303B Burst Function Unit are expansion units, and are installed in the MG3670 series Digital Modulation Signal Generator to generate the I/Q signals for $\pi/4$ DQPSK modulation.

Installing the MG0307A to the mainframe allows modulation signal output conforming to Japan's digital cordless telephones systems (PHS) and U.S.A.'s digital cordless telephones systems (PACS, WCPE).

Installing the MG0307A and the MG0303B enables outputting the burst signal based on each the communication-system channel format.

We guarantee the MG0307A's performance when the MG0307A is combined with the mainframe in the state upon factory-shipment. If it is combined with the MG3670A mainframe, the MG3670A needs to be modified.

1.2 Composition of Operation Manual

This operation manual is composed of five sections. Each section is outlined below.

Section composition	Explanation
SECTION 1 GENERAL	Provides information about product outline, composition of manual, equipment configuration with standard accessories, related unit, and specifications
SECTION 2 BASIC OPERATION	Provides information about basic operation and auxiliary control signals
SECTION 3 DETAILED OPERATIONS	Provides information about operating communication systems and trigger function
SECTION 4 MEASUREMENT	Provides information about typical measurement examples for the digital mobile radio.
SECTION 5 PERFORMANCE TESTS	Provides information about equipment required for executing MG0307A performance tests, setup, and procedure of performance tests

1.3 Equipment Configuration

This paragraph describes the configuration of the MG0307A π/4 DQPSK Modulation Unit and the related unit to expand the function.

1.3.1 Standard configuration

The table below shows the configuration of the MG0307A with the standard accessories:

Table 1-1 Standard Composition

Item	Model / Order No.	Name	Qty.	Remarks
Main instrument	MG0307A	π/4 DQPSK Modulation Unit	1	
Accessories	W0949AE	Operation manual	1	Involves the description of the MG0303B function related to the MG0307A

1.3.2 Unit

The table below shows the related units for the MG3670 series. (The MG0307A not included)

Table 1-2 Expansion Units

Modulation Units for Communication Systems:

Model No.	Name	System to be used
MG0301C	π/4 DQPSK Modulation Unit	PDC[†1], PHP, NADC, TFTS, PDC_H[†2]
MG0302A	GMSK Modulation Unit	GSM, PCN, CT2
MG0305A	GFSK Modulation Unit	DECT

Burst Function Unit: used with the modulation units for Communication Systems

Model No.	Name	System to be used
MG0303B	Burst Function Unit	PDC[†1], PHP, NADC, TFTS, PDC_H[†2], CT2, GSM, PCN, DECT, PACS, PHS, WCPE

[†1] The full rate of Japanese Personal Digital Cellular system is expressed as PDC.

[†2] The half rate of Japanese Personal Digital Cellular system is expressed as PDC_H.

1.4 Specifications

The MG0307A and MG0303B specifications are listed in the following table.

1.4.1 MG0307A π/4 DQPSK Modulation Unit specifications

The MG0307A π/4 DQPSK Modulation Unit specifications are listed in Table 1-3.

Table 1-3 MG0307A π/4 DQPSK Modulation Unit Specifications

Applicable system	PACS, PHS, WCPE
Modulation system	π / 4 DQPSK
Vector error	I/Q signal: ≦ 1.5% rms (at 50 Ω output) RF signal: ≦ 1.8% rms (at ≦ +5 dBm output)
Internal modulation data	Pseudorandom pattern: PN15/PN9 [Free 4-bit repetition pattern (ex: 1010, 1111)] ; PACS, PHS [Free 16-bit repetition pattern (ex: $0F0F_H$, $55AA_H$)] ; WCPE
External modulation data	Data Clock: Covering ±5% of bit rate Data: Digital data synchronized with Data Clock Symbol Clock: Clock specified by Data synchronized with Data Clock [TTL level, BNC connector, polarity selectable]
I/Q signal output	Selectable 50 Ω or CMOS (600 Ω), BNC connector 50 Ω setting: 1 Vp-p ±2% (modulation data: 0000) CMOS setting: Variable in 10% steps over the 10% to 100% range of 1 Vp-p ±2% (modulation data: 0000) Variable offset voltage: 0 to 4 V (1 mV steps)
Adjacent channel leakage power ratio (with MG3670B installed)	For PHS system ≦ −70 dB: 600 kHz offset, ±96 kHz bandwidth ≦ −70 dB: 900 kHz offset, ±96 kHz bandwidth
PACS	Carrier frequency range: 1 to 2250 MHz† Bit rate: 384 kbps Baseband filter: Root Nyquist: $\alpha = 0.5$, Nyquist: $\alpha = 0.5$
PHS	Carrier frequency range: 1 to 2250 MHz† Bit rate: 384 kbps Baseband filter: Root Nyquist: $\alpha = 0.5$, Nyquist: $\alpha = 0.5$
WCPE	Carrier frequency range: 5 to 2250 MHz† Bit rate: 1152 kbps Baseband filter: Root Nyquist: $\alpha = 0.5$, Nyquist: $\alpha = 0.5$

† The upper limit of carrier frequency conforms to the specification of the MG3670 series.

1.4.2 MG0303B Burst Function Unit specifications

Table 1-4 lists the MG0303B Burst Function Unit specifications for (PACS / PHS / WCPE) when used with the MG0307A.

Table 1-4 MG0303B Burst Function Unit Specifications (1/2)

Applicable communication system		PACS, PHS, WCPE (with MG0307A)
Modulation signal	Internal data mode	TDMA framing specified for each system; modulation in each time slot using any Internal data mode
	Internal modulation data	Pseudorandom pattern: PN15/PN9†(for device) Specified pattern based on communication channel format specified for each system: Up/down communication channel, VOX control TCH, DATA, FC section consists of pseudorandom pattern (PN15/PN9)†1
	External data mode	Data Clock: Covering ±5% of bit rate Data: Digital data synchronized with Data Clock Symbol Clock: Clock specified by Data synchronized with Data Clock [TTL level, BNC connector, polarity selectable]
Auxiliary signal input	Burst trigger input	Outputs burst wave synchronized with trigger input signal of burst repetition. Input period: burst repetition rate ±1 symbol [TTL level, BNC connector (rear panel), polarity selectable]
	Burst gate input	Outputs burst waveform corresponding to input signal width. Input signal width: ≧14 symbols, period: ≧22 symbols [TTL level, BNC connector (rear panel), polarity selectable]
Auxiliary signal output	Burst trigger output	Outputs 1-symbol width pulse at same cycle as burst waveform output. [TTL level, BNC connector (rear panel), polarity selectable]
	Pattern sync output	Following outputs selectable at internal modulation: PN Clock: Data clock corresponding to pseudorandom pattern part PN Gate: Gate signal corresponding to pseudorandom pattern part RF Gate: Signal for controlling pulse modulator in accordance with burst signal output [TTL level, BNC connector (rear panel)]
	Burst gate output	Outputs gate signal corresponding to burst waveform output at internal modulation. [TTL level, BNC connector (rear panel), polarity selectable]
RF output	Burst on/off ratio	≧75 dB (+5 dBm output, PACS, PHS), ≧70 dB (+5 dBm output, WCPE)
	Rise/fall time	Equivalent to 2 symbols

† Pseudorandom pattern in each has different phase, and its pattern within the TCH segment of slots is continuous.

Table 1-4 MG0303B Burst Function Unit Specifications (2/2)

Memory	Pattern memory	100 patterns (store and recall of internal modulation pattern data)
PACS	Burst repetition period	2.5 ms
	Slot configuration	For device, up/down communication channel
	Output slot select	On/off selectable for any slots of Slot 0 to Slot 7 (excluding all slots off)
	Edit function	DE/SC/R/SYC/PCC: Any data, FC: PN9/PN15 All 0/All 1 selectable
PHS	Burst repetition period	5 ms
	Slot configuration	For device, up/down communication channel, VOX control, synchronous burst
	Output slot select	On/off selectable for any slots of Slot 1 to Slot 4 (excluding all slots off)
	Edit function	UW/SA: Any data, TCH: PN9/PN15 selectable
	Scramble function	TCH + CRC, scramble and secret scramble on/off, any scramble code setting
WCPE	Burst repetition period	10 ms
	Slot configuration	For device, up/down communication channel (P00, P32, P80, P08)
	Output slot select	On/off selectable for any slots of Slot 0 to Slot 11 ; downlink line On/off selectable for any slots of Slot 12 to Slot 23 ; uplink line
	Edit function	Data selectable for S, H, T, and DATA On/off selectable for Z

SECTION 2
BASIC OPERATION

This section describes basic operation procedures for the MG0307A $\pi/4$ DQPSK Modulation Unit and the MG0303B Burst Function Unit and their auxiliary signals. See Section 3 on how to use the modulation patterns and trigger signals for each system.

TABLE OF CONTENTS

2.1 Screen Transition 2-3

2.2 Setting the Modulation Parameters 2-4

2.3 Setting Internal Modulation Data 2-7

2.4 Internal Modulation Data Memory 2-9
- 2.4.1 Saving internal modulation data 2-9
- 2.4.2 Recalling internal modulation data 2-13
- 2.4.3 Deleting internal modulation data 2-14
- 2.4.4 Listing internal modulation data 2-16

2.5 I, Q Signal Outputs 2-17

2.6 Auxiliary signal outputs 2-19
- 2.6.1 Data, data clock and symbol clock signals 2-19
- 2.6.2 Pattern sync signal 2-19
- 2.6.3 Burst gate signal 2-22

2.7 Auxiliary Inputs Signal 2-24
- 2.7.1 Data, data clock and symbol clock signals 2-24
- 2.7.2 Burst gate signal 2-24

2.8 Symbol Adjust Function 2-25

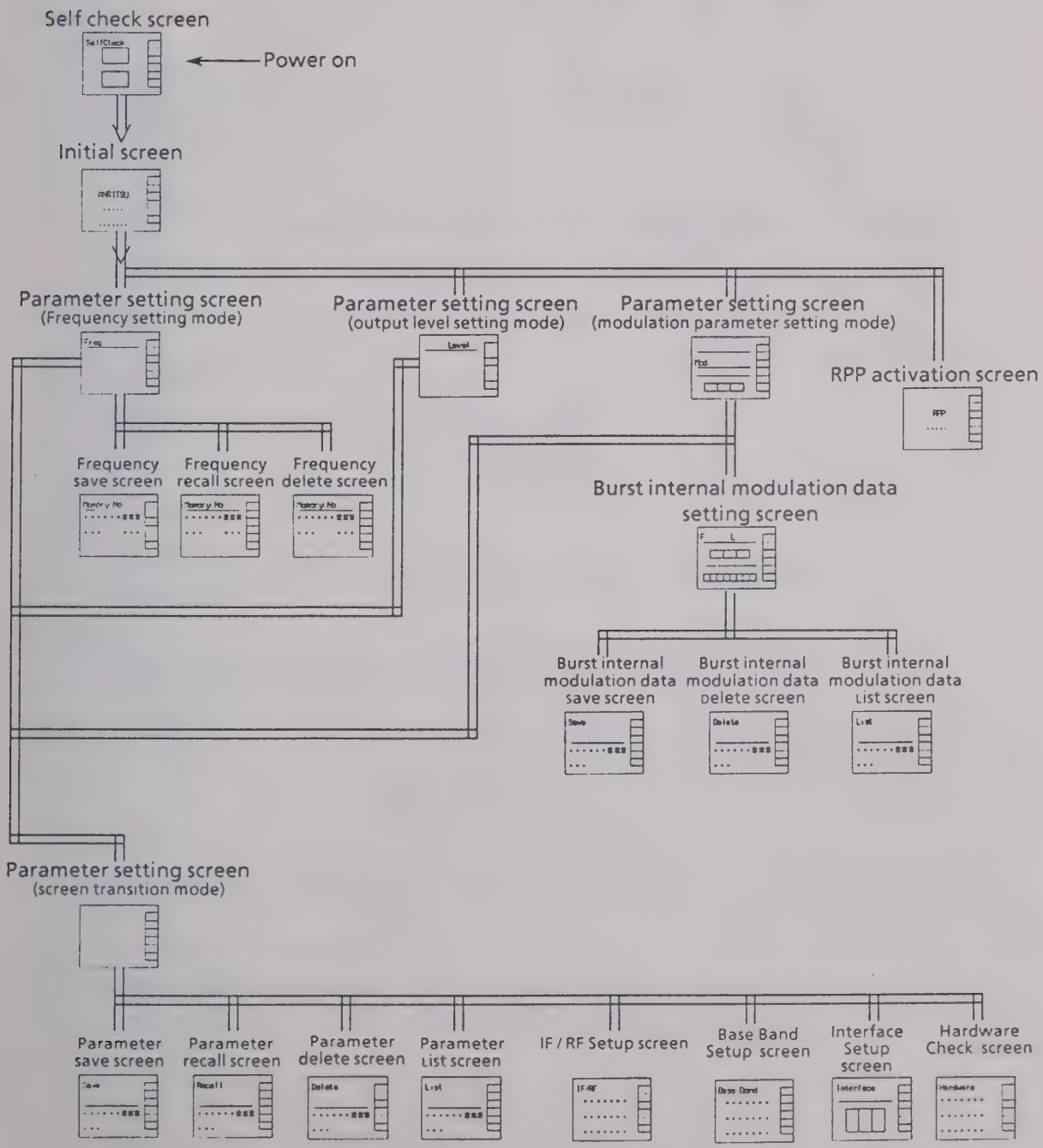
2.9 Phase Encode Function 2-26

(Blank)

SECTION 2
BASIC OPERATION

2.1 Screen Transition

The display screen switches as shown below.



2.2 Setting the Modulation Parameters

(1) Screen

When the Main Function section Mod key on the front panel is pressed, the parameter setting screen (modulation parameter setting mode) appears.

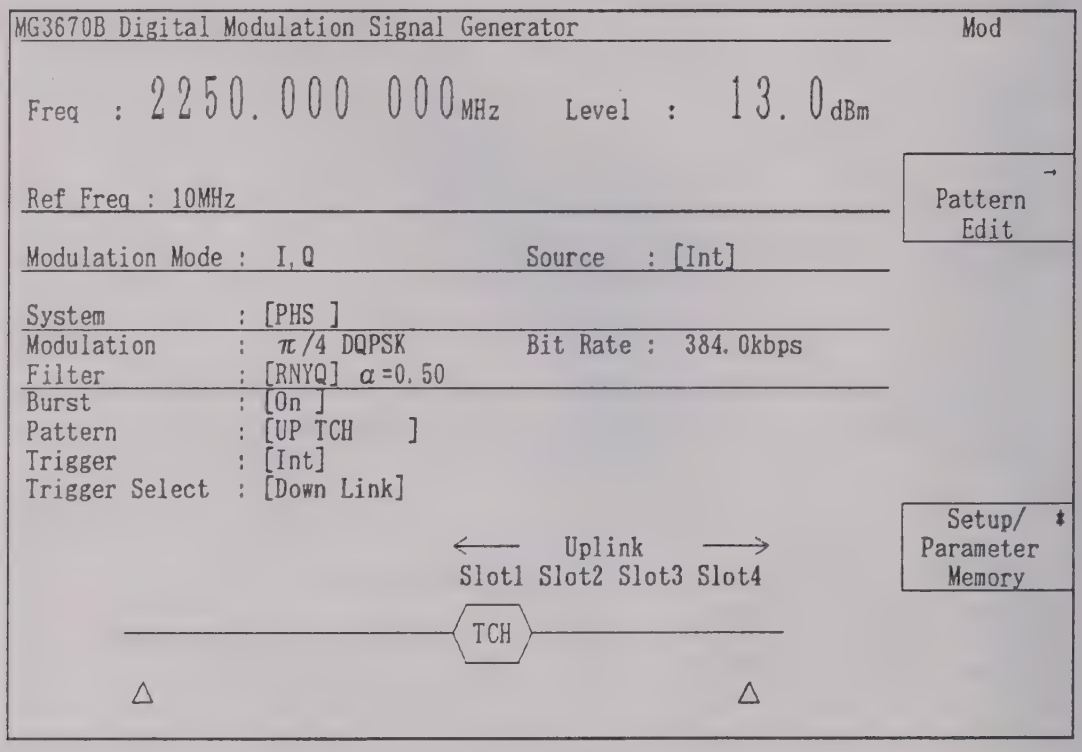


Fig. 2-1 Parameter Setting Screen (modulation parameter setting mode)

Use the Cursor keys to set the following parameters in this screen.

- I, Q signal input ..... Source
- Communication system ..... System
- Baseband filter ..... Filter
- Phase Encode ..... Phase Encode
- Burst function ..... Burst
- Internal modulation data ..... Pattern
- Burst trigger input ..... Trigger
- Burst trigger position ..... Trigger Select

Note: Trigger Select can be set when the communication system is PHS.

(2) Setting parameters

■ Source (Int / Ext)

Sets the I, Q signals to internal (Int) or external (Ext).

Initial setting: Int

■ System

Select one of the three communication systems; PACS / PHS / WCPE. When the communication system is selected, the modulation method, roll-off rate (a), and bit rate are set as shown below.

Initial setting: PACS (does not affect the Preset key)

Communication system	Modulation method	Roll-off rate	Bit rate
PACS	π / 4 DQPSK	$\alpha = 0.5$	384 kbps
PHS	π / 4 DQPSK	$\alpha = 0.5$	384 kbps
WCPE	π / 4 DQPSK	$\alpha = 0.5$	1152 kbps

■ Filter (NYQ / RNYQ)

Nyquist (NYQ) or Root-Nyquist (RNYQ) can be selected as the baseband filter.

Initial setting: Root-Nyquist (RNYQ)
The roll-off rate (α) is fixed according to the communication system.

■ Phase Encode (Normal/ Inverse)

Normally use the normal mode. Selecting the inverse mode inverts the right and left of modulation wave spectrum from the carrier frequency. For detail, refer to Paragraph 3.9.

■ Burst (On / Off)

The burst function can set to On when a burst function unit (MG0303B) is installed.

Initial setting: Off

■ Pattern

The following internal modulation data can be set:
When data of BaseBand Setup screen is externally input, Pattern is not displayed.

- When the burst function is on: Standard internal modulation data of each communication system (For details on the internal modulation data of each communication system, see Section 4.)
  Data stored in the internal modulation data memory (For details, see 3.4 Internal modulation data memory)
- When burst function is off: PN9, PN15 and any 4-bit data (0000 to 1111), any 16-bit data (0000_H to $FFFF_H$)

■ Trigger (Int / Ext)

Sets the burst trigger to either internal (Int) or external (Ext) when the burst function is on.

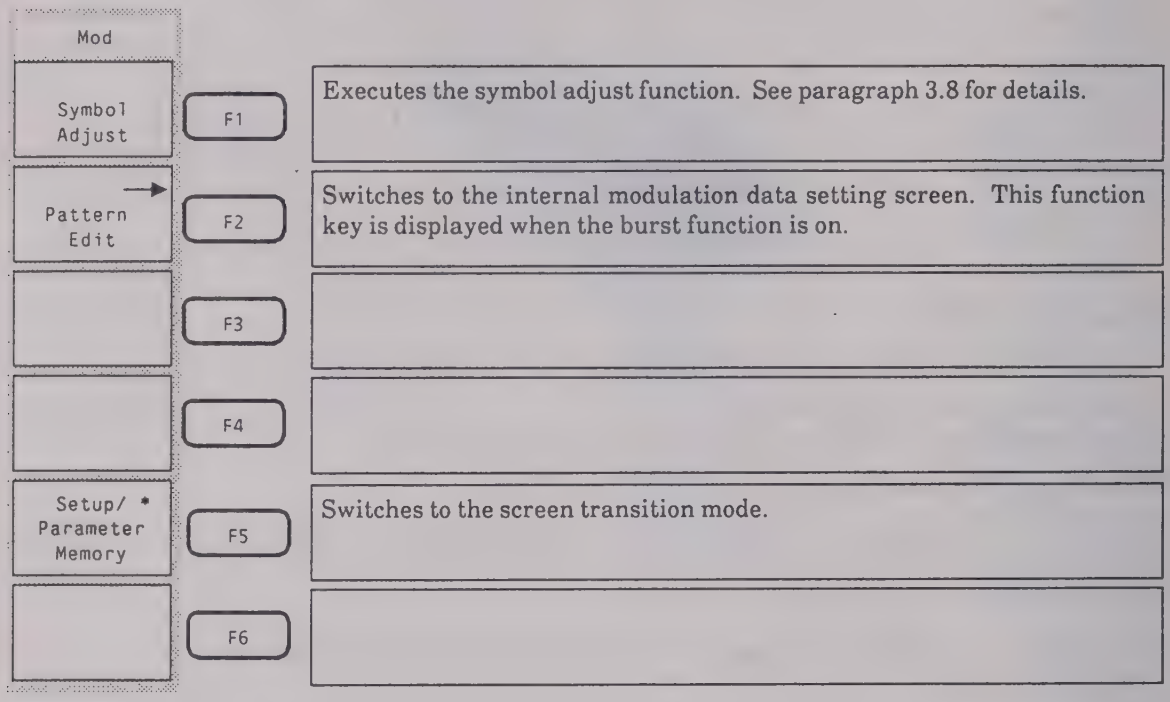
Initial setting: Int

■ Trigger Select (Uplink / Downlink)

Sets the burst trigger position of the PHS system to either Uplink or Downlink when the burst function is on.

Initial setting: Downlink

(3) Function keys



2.3 Setting Internal Modulation Data

(1) Screen

The internal modulation data setting screen is displayed when the 'Pattern Edit' F2 soft key shown in the parameter setting screen (modulation parameter setting mode) is pressed while the burst function is on.

The standard internal modulation data set in Pattern in the modulation parameter setting screen is displayed in this screen.

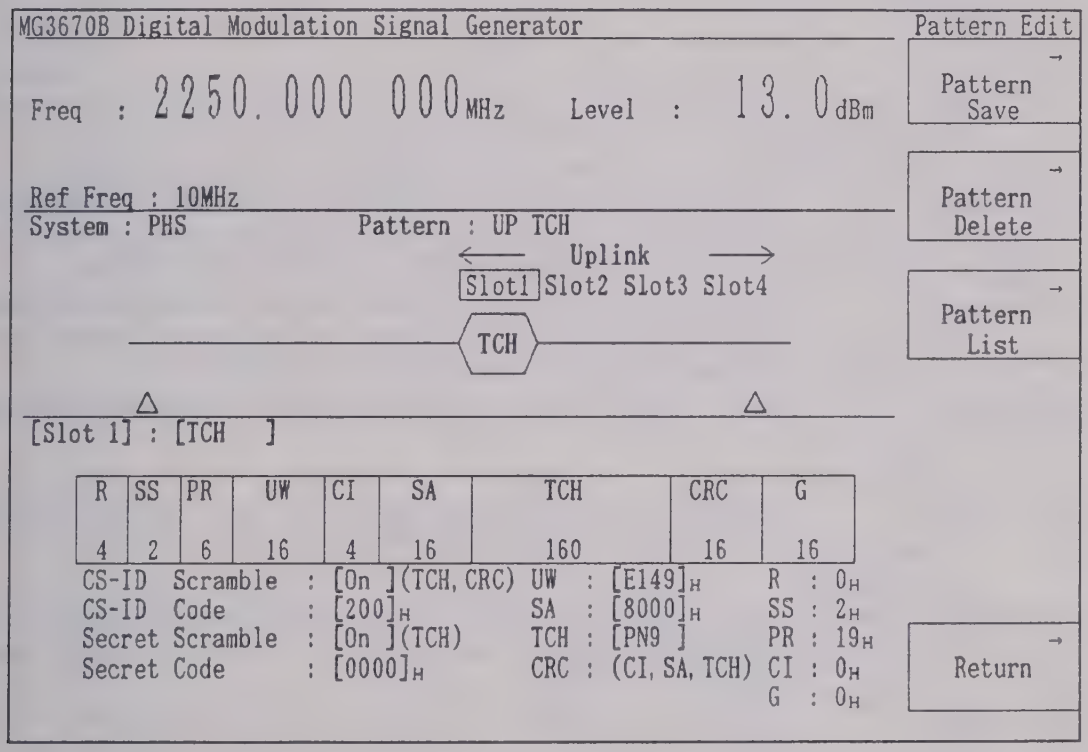


Fig. 2-2 Internal Modulation Data Setting Screen (PDC system)

Note: *The internal modulation data cannot be set if there is no burst function unit (MG0303B) installed.*

(2) Set parameters

■ Slot number

Selects the numbers of the desired slots.

PACS: Slot 0 to Slot 7
PHS: Slot 1 to Slot 4
WCPE: Slot 0 to Slot 23

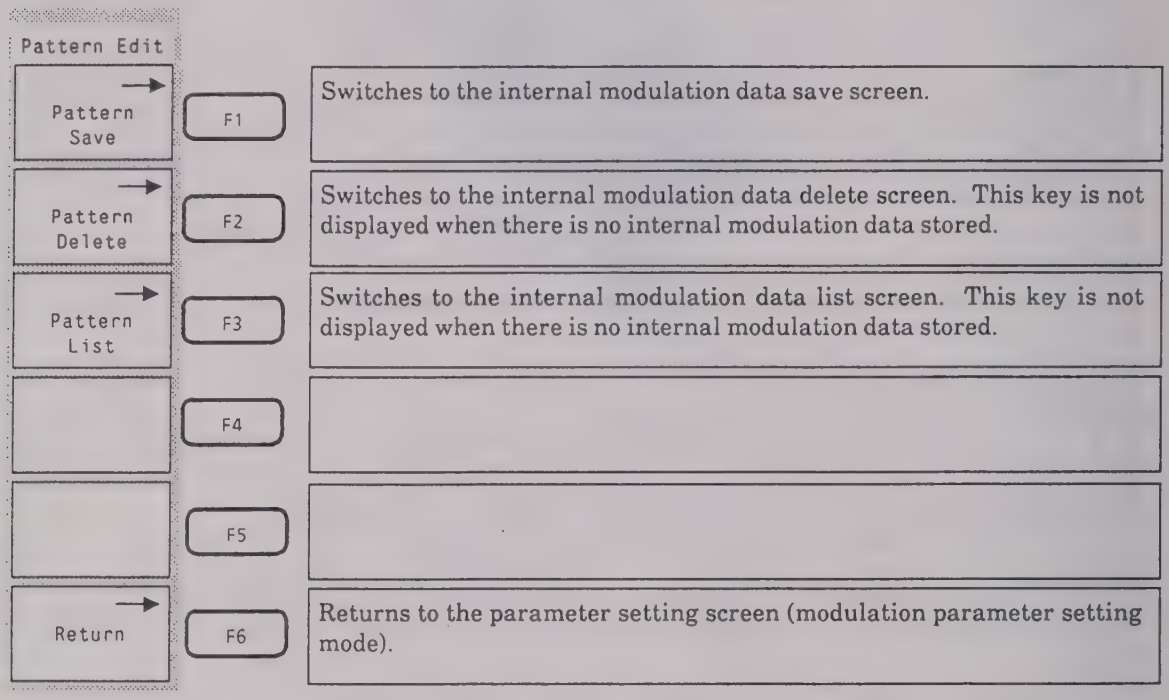
■ Slot

Selects the applicable slot. The selectable slot depends on the standard internal modulation data set in Pattern of each communication system. For details on the internal modulation data of each communication system, see Section 3.

■ Modulation data

Sets the modulation data of a slot. The selectable types and ranges of modulation data differ from slot to slot. For details on the internal modulation data of each communication system, see Section 4.

(3) Function keys


Pattern Edit
Pattern Save
F1
Switches to the internal modulation data save screen.
Pattern Delete
F2
Switches to the internal modulation data delete screen. This key is not displayed when there is no internal modulation data stored.
Pattern List
F3
Switches to the internal modulation data list screen. This key is not displayed when there is no internal modulation data stored.
F4
F5
Return
F6
Returns to the parameter setting screen (modulation parameter setting mode).

2.4 Internal Modulation Data Memory

Modulation data set in the internal modulation data setting screen can be stored into, retrieved, deleted and listed from memory. Each of the memory operations are discussed in detail below.

2.4.1 Saving internal modulation data

When the 'Pattern Save' F1 soft key is pressed in the internal modulation data setting screen, the internal modulation data save screen appears. Specify the memory location number using the data keys, rotary knob, Step keys or Cursor keys and press the Set or Enter key to store the set data.

Memory location number range: 0 to 99

(1) Screen

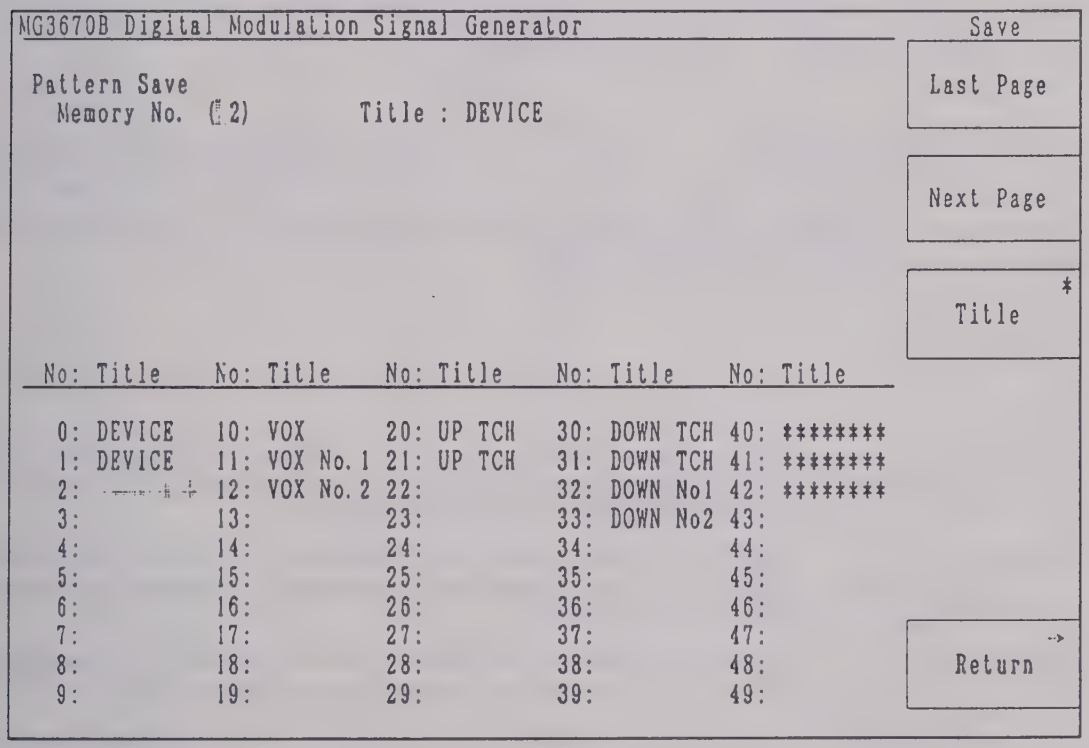

MG3670B Digital Modulation Signal Generator
Save
Pattern Save
Memory No. (2)
Title : DEVICE
Last Page
Next Page
Title
No: Title No: Title No: Title No: Title No: Title
0: DEVICE 10: VOX 20: UP TCH 30: DOWN TCH 40: ********
1: DEVICE 11: VOX No. 1 21: UP TCH 31: DOWN TCH 41: ********
2: 12: VOX No. 2 22: 32: DOWN No1 42: ********
3: 13: 23: 33: DOWN No2 43:
4: 14: 24: 34: 44:
5: 15: 25: 35: 45:
6: 16: 26: 36: 46:
7: 17: 27: 37: 47:
8: 18: 28: 38: 48:
9: 19: 29: 39: 49:
Return

Fig. 2-3 Internal Modulation Data Save Screen

Initial memory location number: Currently available location having the smallest number

If data is already stored in the specified location, a Yes/No window appears for confirmation purposes. Press the Set key to overwrite the current data. After storing the data, the internal modulation data setting screen is redisplayed.

Example: Stores modulation data in memory location 10.

Step	Action	Verification
1	Mod †	Sets the modulation parameter setting mode and lights the Mod key's LED indicator.
2	Pattern Edit F3	Displays the internal modulation data setting screen.
3	Pattern Save F1	Displays the internal modulation data saving screen.
4	1 0 Set	Specifies memory location 10 and stores internal modulation data in that location.

† There is no need to press the Mod key if its indicator is already lit.

(3) Function keys

Save		
Last Page	F1	Displays the previous page of the current data list. No operation is performed when there is no previous page.
Next Page	F2	Displays the next page of the current data list. Nothing is done when there is no next page.
* Title	F3	Displays the title input window and related function keys.
	F4	
	F5	
→ Return	F6	Returns to the internal modulation data setting screen.

■ Inputting a title

A title up to eight characters long can be entered when storing internal modulation data. "********" is displayed in the title field when no title is specified.

(1) Screen

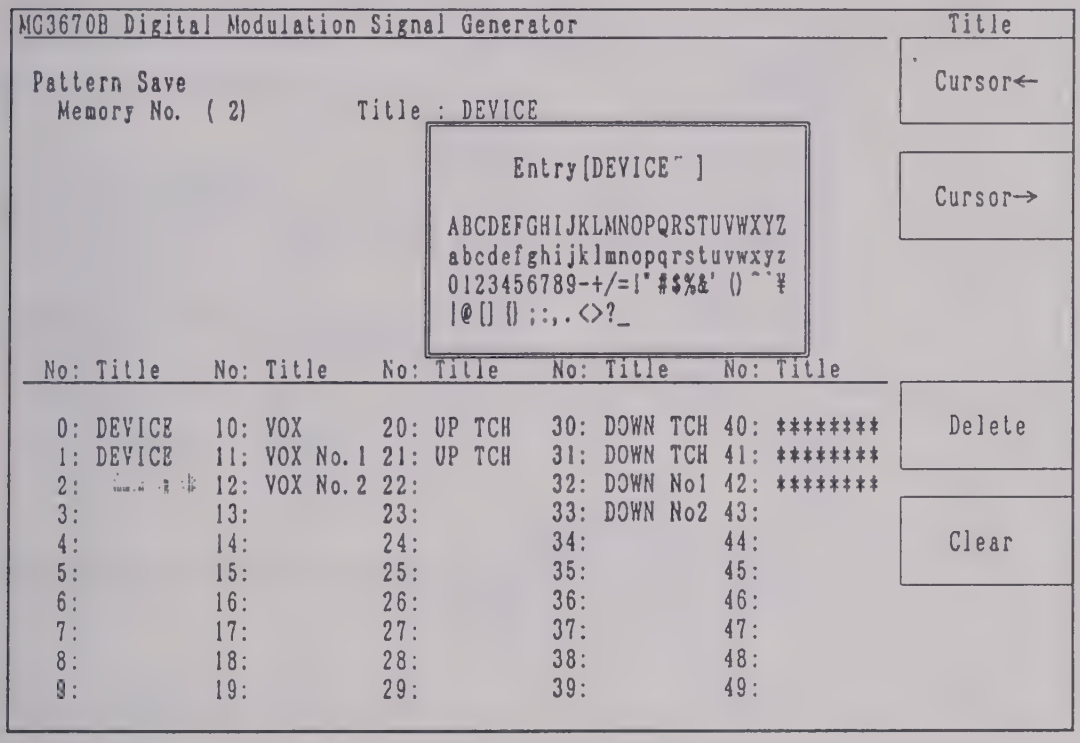
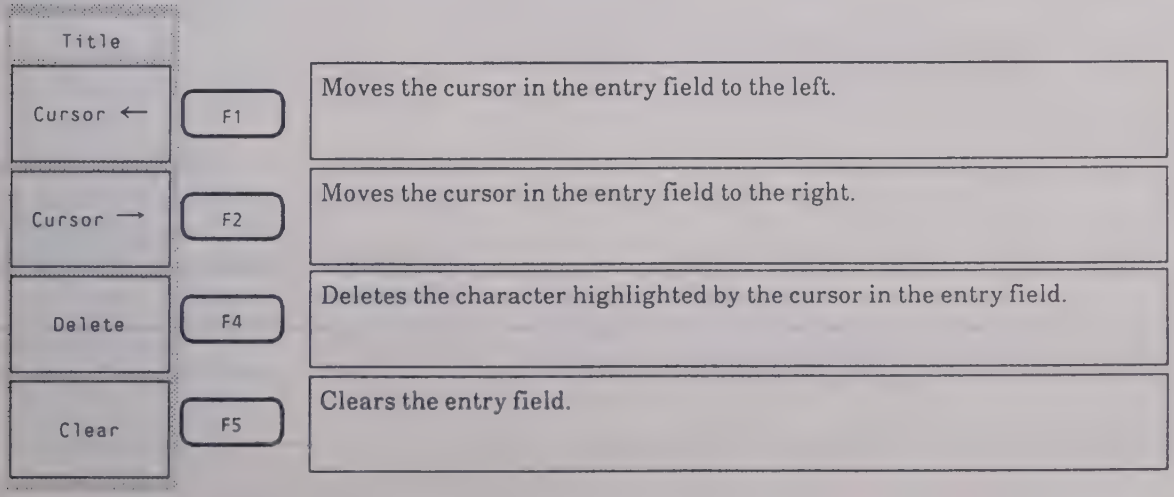


Fig. 2-4 Internal modulation data save screen (title input window)

(2) Function keys



Example : Inputs the title 'Anritsu'.

Step	Action	Verification
1	Mod †	Switches to modulation parameter setting mode and lights the Mod key's LED indicator.
2	Pattern Edit F2	Switches to the internal modulation data setting screen.
3	Pattern Save F1	Switches to the internal modulation data save screen.
4	Title F3	Opens the window for setting the title.
5	Clear F5	Clears the title entry field.
6	Cursor ← F1, Cursor → F2	Moves the cursor within the entry field.
7	Cursor keys or rotary knob	Selects the characters from the character list.
8	Enter	Enters the selected character in the Entry field.
9	BS	Deletes an erroneously entered character.
10	Repeat steps 6, 7 and 8 until 'Anritsu' is completely entered.	
11	Set	Closes the title input window after inputting the title. (After inputting the title, specify the memory location number where internal modulation data will be stored.)

† There is no need to press the Mod key if its LED indicator is already on.

Note: *The title can also be entered using the data keys.*

2.4.2 Recalling internal modulation data

Data saved in the internal modulation data save screen can be retrieved through the Pattern setting in the parameter setting screen (modulation parameter setting mode).

(1) Screen

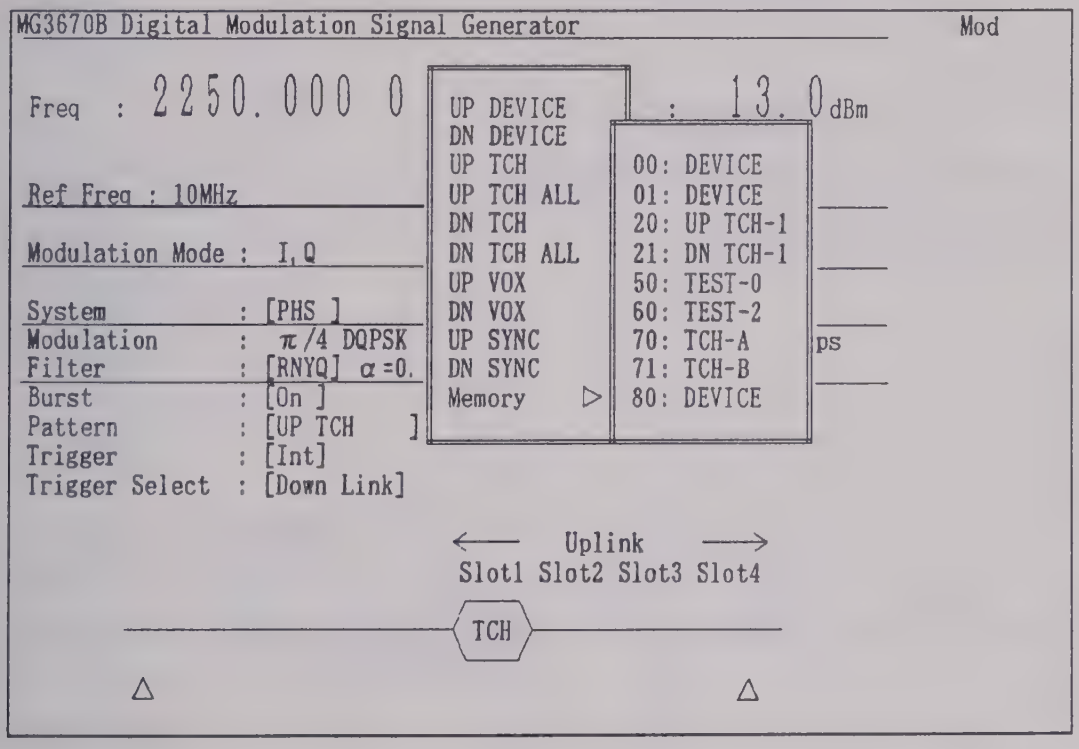
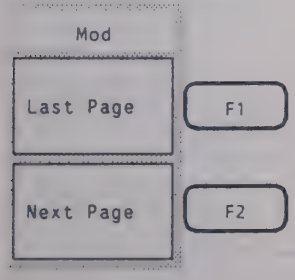


Fig. 2-5 Parameter Setting Screen (modulation parameter setting mode, Pattern setting window)

If internal modulation data is stored in memory, 'Memory▷' is displayed in the Pattern setting window in the parameter setting screen (modulation parameter setting mode). When this is selected, a sub-window opens and data stored in memory are displayed.

When the Set key is pressed and the pattern selected, both windows close simultaneously. Press the Cancel key to close the sub-window only.

(2) Function keys



Last Page (F1)	Displays the previous page in the sub-window. No operation is performed when there is no previous page.
Next Page (F2)	Displays the next page in the sub-window. No operation is performed when there is no previous page.

2.4.3 Deleting internal modulation data

When the 'Pattern Delete' F2 soft key is pressed in the internal modulation data setting screen, the internal modulation data delete screen appears. Use the data keys, rotary knob, Step keys and Cursor keys to specify the memory number and then press the Set and Enter keys. A Yes/No window then appears for verification. Select Yes to delete the data.

Initial memory location number: Currently saved memory location having the smallest number

(1) Screen

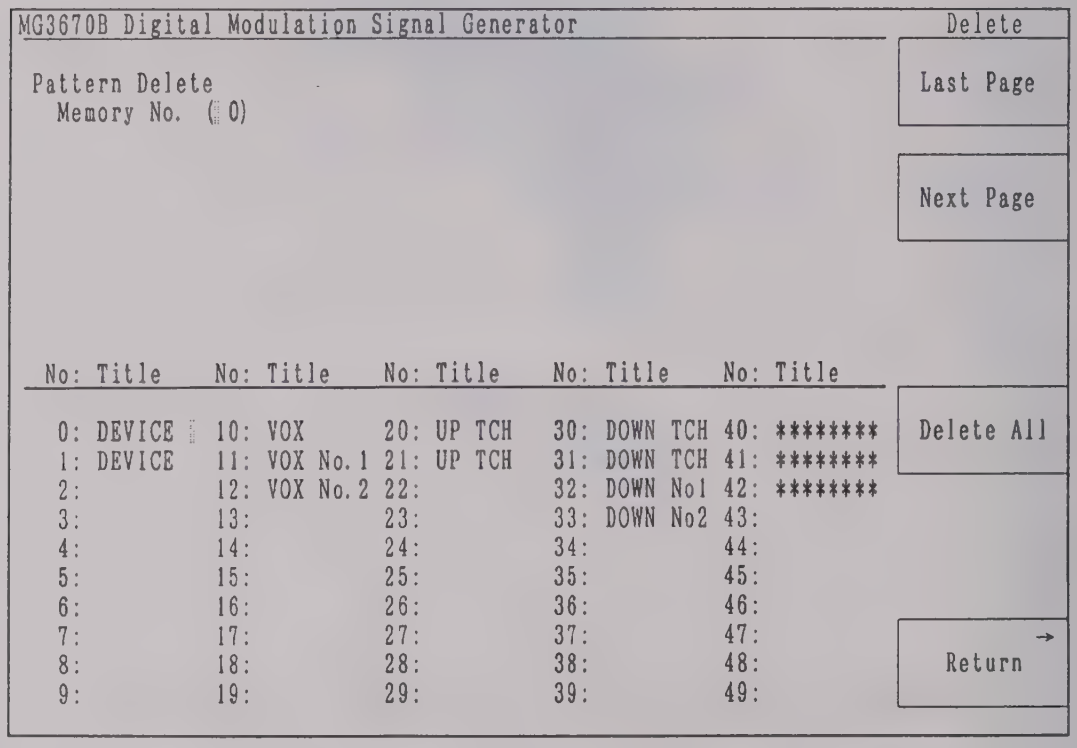

MG3670B Digital Modulation Signal Generator
Delete
Pattern Delete
Memory No. (0)
Last Page
Next Page
No: Title No: Title No: Title No: Title No: Title
0: DEVICE 10: VOX 20: UP TCH 30: DOWN TCH 40: ********
1: DEVICE 11: VOX No.1 21: UP TCH 31: DOWN TCH 41: ********
2: 12: VOX No.2 22: 32: DOWN No1 42: ********
3: 13: 23: 33: DOWN No2 43:
4: 14: 24: 34: 44:
5: 15: 25: 35: 45:
6: 16: 26: 36: 46:
7: 17: 27: 37: 47:
8: 18: 28: 38: 48:
9: 19: 29: 39: 49:
Delete All
Return

Fig. 2-6 Parameter Setting Screen (modulation parameter setting mode, pattern data deletion)

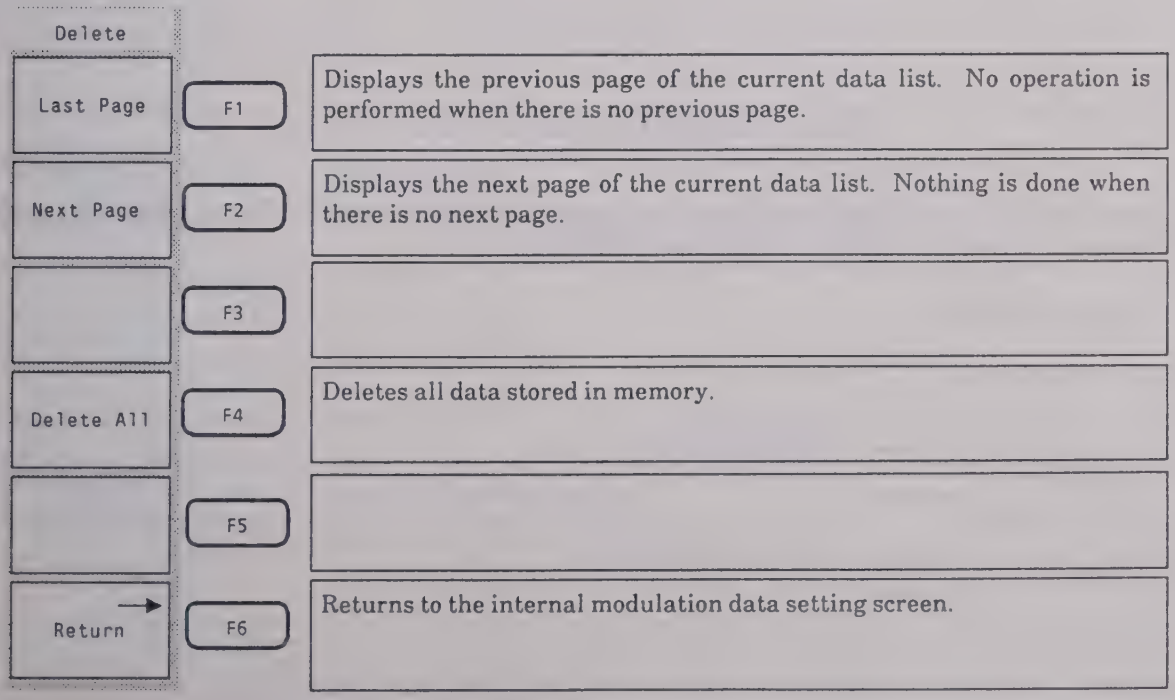
To delete all data in memory, press the 'Delete All' F4 soft key. 'All' is displayed in the memory number field and all data set in the list are reversely highlighted. A Yes/No window then appears for verification purposes. Press Yes to delete all of the data sets.

Example: Deletes the internal modulation data in memory location 10.

Step	Action	Verification
1	Mod†	Switches to the modulation parameter setting mode and the Mod key's LED indicator lights.
2	Pattern Edit + F2	Switches to the internal modulation data setting screen.
3	Pattern Delete + F2	Switches to the internal modulation data delete screen.
4	1 0 Set	Specifies memory location 10. (A Yes/No window opens for verification.)
5	Cursor < Set	Select Yes to delete the data.

† There is no need to press the Mod key if its indicator is already lit.

(2) Function keys


Delete
Last Page
F1
Displays the previous page of the current data list. No operation is performed when there is no previous page.
Next Page
F2
Displays the next page of the current data list. Nothing is done when there is no next page.
F3
Delete All
F4
Deletes all data stored in memory.
F5
Return
F6
Returns to the internal modulation data setting screen.

2.4.4 Listing internal modulation data

When the 'Pattern List' F3 soft key is pressed in the internal modulation data setting screen, the internal modulation data list screen appears. Use the data keys, rotary knob, Step keys and Cursor keys to specify the memory location number and then press the Set or Enter key to display in a window the internal modulation data stored in that location.

Initial memory location number: Currently saved memory location having the smallest

(1) Screen

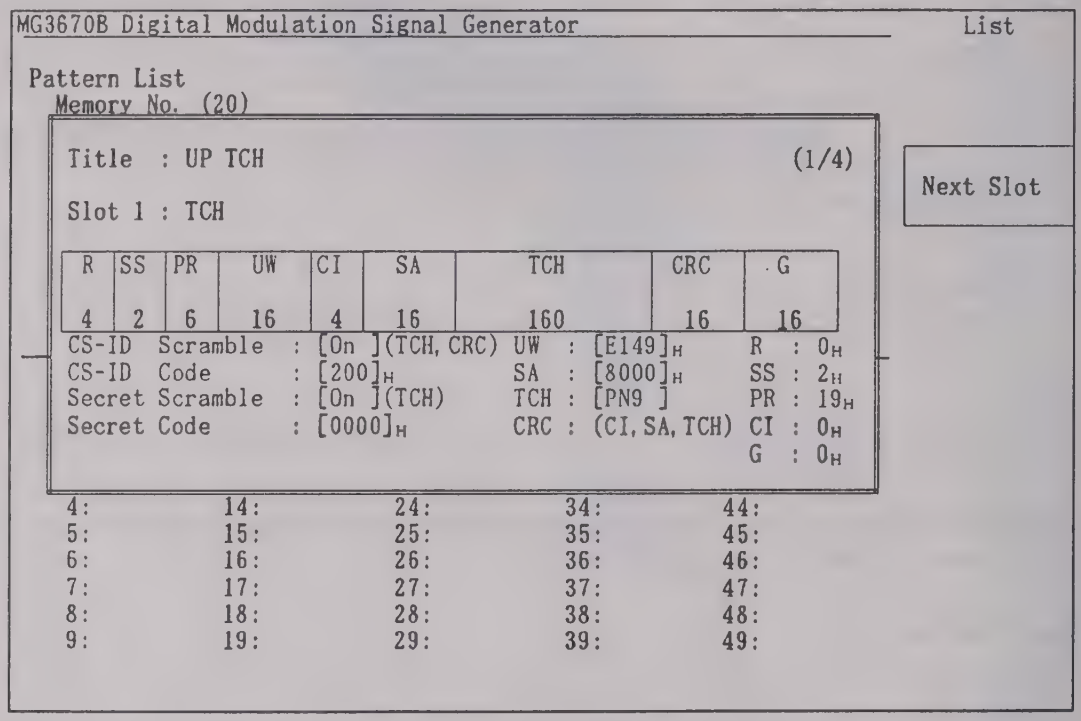
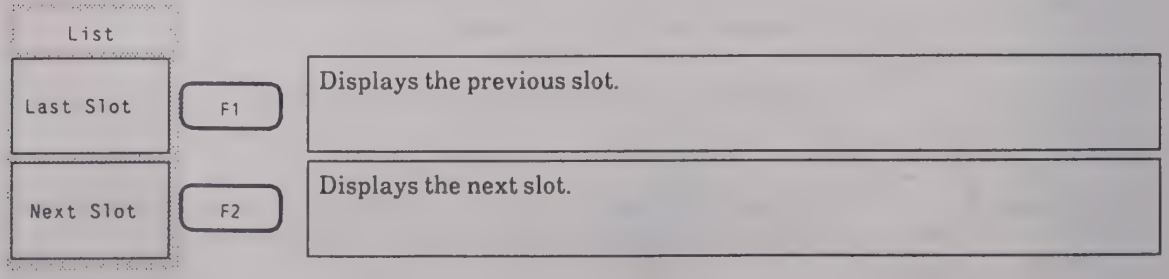

MG3670B Digital Modulation Signal Generator
List
Pattern List
Memory No. (20)
Title : UP TCH
(1/4)
Slot 1 : TCH
Next Slot
R SS PR UW CI SA TCH CRC G
4 2 6 16 4 16 160 16 16
CS-ID Scramble : [On](TCH, CRC)
CS-ID Code : [200]H
Secret Scramble : [On](TCH)
Secret Code : [0000]H
UW : [E149]H
SA : [8000]H
TCH : [PN9]
CRC : (CI, SA, TCH)
R : 0H
SS : 2H
PR : 19H
CI : 0H
G : 0H
4: 14: 24: 34: 44:
5: 15: 25: 35: 45:
6: 16: 26: 36: 46:
7: 17: 27: 37: 47:
8: 18: 28: 38: 48:
9: 19: 29: 39: 49:

Fig. 2-7 Internal Modulation Data List Screen

Internal modulation data is displayed per slot; Use the 'Last Slot' F1 and 'Next Slot ' F2 soft keys to select the slot. Press the Set or Cancel key to close the window.

(2) Function keys



2.5 I, Q Signal Outputs

The I, Q signal outputs are always produced regardless of the I, Q modulation signal source setting (Int or Ext). The I, Q signals are described as follows:

Setting		I, Q signal output
Modulation	Source	
On	Int	Outputs I,Q signals corresponding to the currently set modulation.
	Ext	Outputs I,Q signals immediately before the source is set to Ext.
Off	——	Outputs a DC voltage signal for non-modulated signals.

Note: *Only the DC voltage signal for non-modulated signals is output for models that are not equipped with a modulation unit.*

(1) Setting the output level

The output level can be set within the range shown in the table below. However, the input and output settings will be the same. For details, refer to the 'Panel Operating Instructions part ' in the MG3670 series (main instrument) operation manual.

I, Q Level	Impedance		Input/Output level	Offset voltage
	Input	Output		
50 Ω 500 mV selected	50 Ω	50 Ω	500 mVrms (Fixed)	0 mV (Fixed)
CMOS selected	100 kΩ	600 Ω	50 to 500 mVrms , 50 mVrms step	0 to 4000mV, 1 mV step

■ **Defining the output levels of the I, Q signals:**

Output level is $\sqrt{I^2 + Q^2}$ for '0000' pattern, terminated voltage;

terminated impedance is as follows:

When 50 Ω, 500 mV is selected: 50 Ω
When CMOS is selected: 600 Ω

Note: *For details on the I, Q signals input level, refer to the 'Panel Operating Instructions part ' in the MG3670 series (main instrument) operation manual.*

(2) I, Q output balance, offset and phase adjustment functions

When the I, Q output trimmer function is set to On, the adjustment function is activated. For details on the setting method, refer to the 'Panel Operating Instructions part ' in the MG3670 series (main instrument) operation manual.

■ Balance adjustment function

The balance adjustment function fixes the amplitude of the Q signal and varies the amplitude of the I signal within ±20%.

■ Offset adjustment function

The offset adjustment function adds an offset voltage ranging within ±0.1 V to the I and Q output signals. (The I signal offset voltage can be independently adjusted from the Q signal offset voltage.)

■ Phase adjustment function

The phase adjustment function shifts the phase of the I signal within a ±10° range. This shift operation can be expressed in an equation as follows:

$I_{OUT} = I \cdot \cos\theta + Q \cdot \sin\theta$

$Q_{OUT} = Q$

I_{OUT}:	I signal output when the I and Q signal adjustment function is On
Q_{OUT}:	Q signal output when the I and Q signal adjustment function is On
I:	I signal output when the I and Q signal adjustment function is Off
Q:	Q signal output when the I and Q signal adjustment function is Off
θ:	Phase shift angle; Can be varied within ±10° with the trimmer

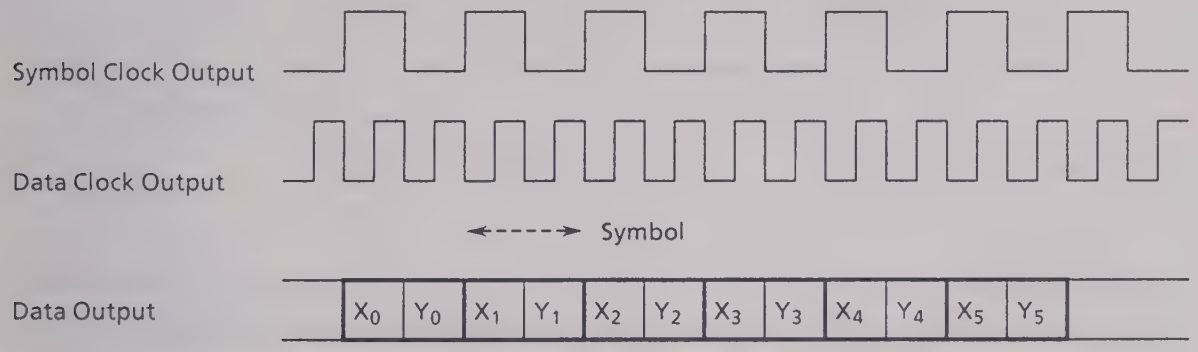
Note: *The functions described above cannot be independently set On or Off.*

2.6 Auxiliary signal outputs

This section explains the control signals output from the MG3670 series rear panel. For details on the IQ DC offset, refer to the 'Panel Operating Instructions part ' in the MG3670 series (main instrument) operation manual.

2.6.1 Data, data clock and symbol clock signals

The output timings of the Data, Data Clock and Symbol Clock signals are shown below. In the figure, the polarities of the signals are expressed as positive or rising edge.



The symbol consists of Xn and Yn, where Xn indicates data that occurs before Yn.

2.6.2 Pattern sync signal

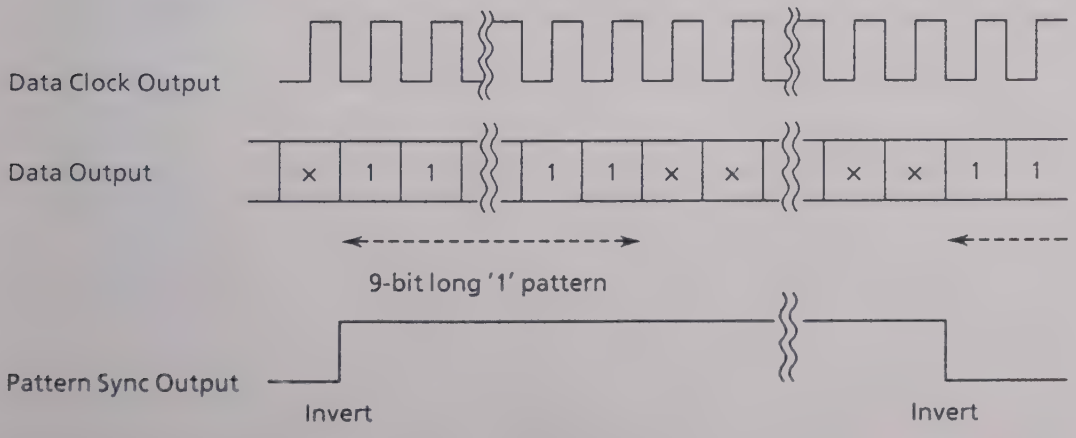
The Pattern Sync output signal that is produced depends on whether the burst function is On or Off. This is explained as follows:

(1) When burst function is Off:

When the burst function is off, the Pattern Sync Output signal allows a signal synchronized with the output pattern to be output.

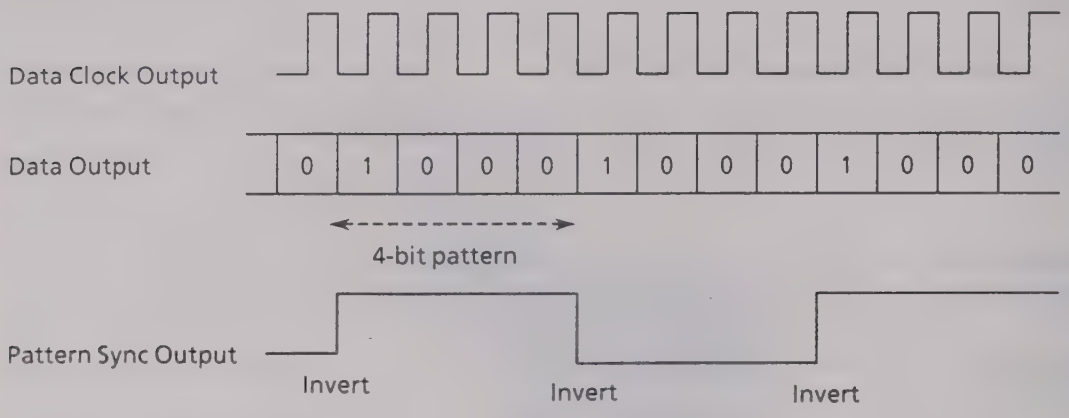
■ When PN pattern is selected

When PN9 is selected, an invert signal is output at the beginning of a pattern consisting of nine contiguous '1' bits. When PN15 is selected, an invert signal is output at the beginning of a pattern consisting of fifteen contiguous '0' bits. The output signal when PN9 is selected is shown below:



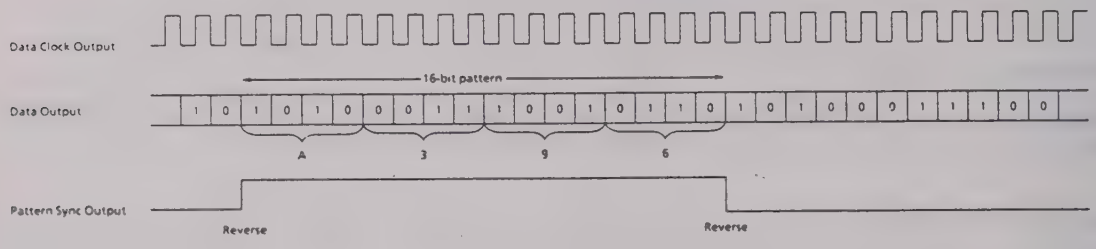
■ When 4-bit pattern is selected:

An invert signal is output at the beginning of the 4-bit pattern. The figure is based on a '1000' 4-bit pattern.



■ When 16-bit pattern is selected:

A reversed signal is output at the beginning of the 16-bit pattern. The figure below shows when the 16-bit pattern is set to " A396 " $_{H}$.


Data Clock Output
16-bit pattern
Data Output
1 0 1 0 1 0 0 0 1 1 1 0 0 1 0 1 1 0 1 0 1 0 0 0 1 1 1 0 0
A
3
9
6
Pattern Sync Output
Reverse
Reverse

(2) When the burst function is On

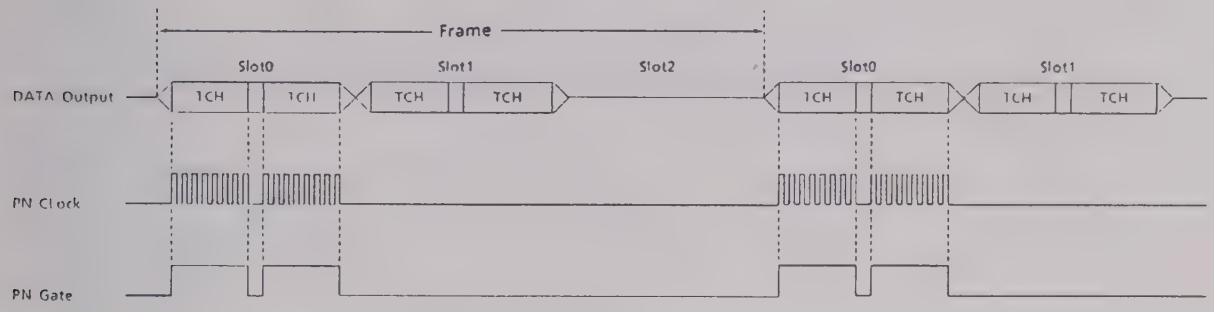
The Pattern Sync Output Signal allows when the burst function is On, a control signal synchronized with the frames to be output.

■ When the PN clock is selected

The clock signal of the pseudorandom pattern of the first output slot in the frame is output.

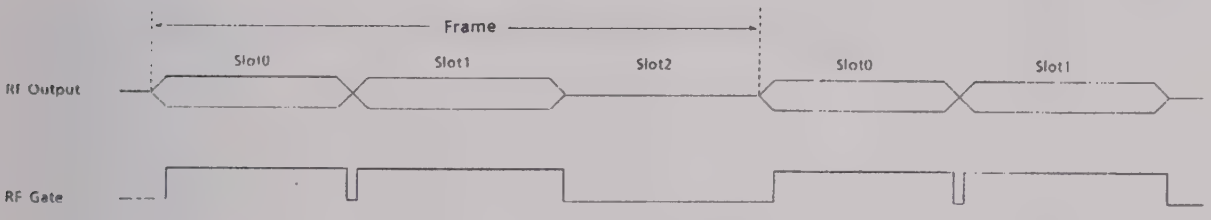
■ When the PN gate is selected

The gate signal of the pseudorandom pattern of the first output slot in the frame is output.

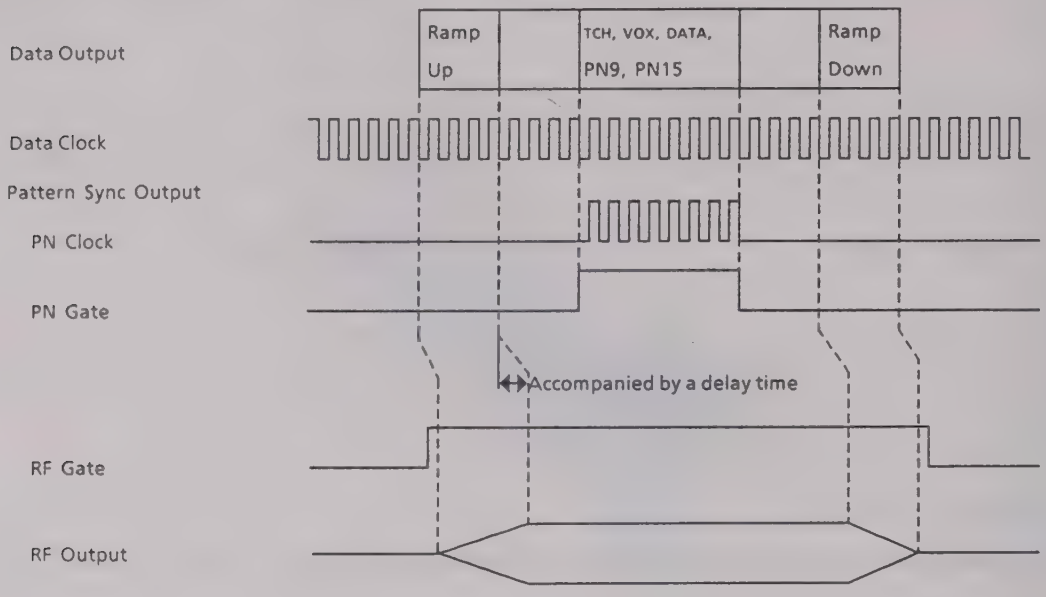


■ When the RF gate is selected

A control signal from the pulse modulation unit inside the main instrument is output.

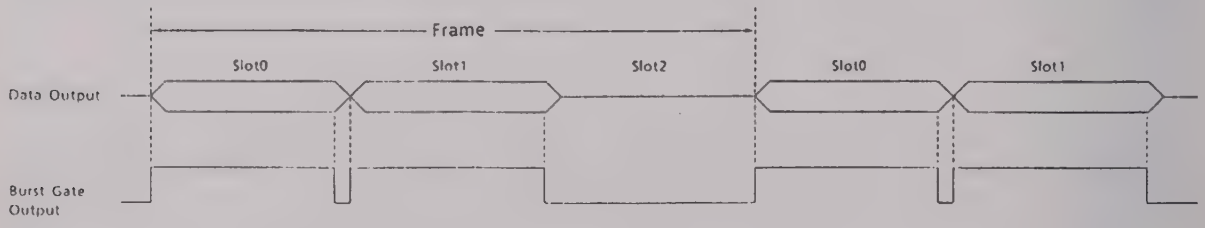


The details about the slot are shown in the figure below. The format of the slot in this figure is for explanation purposes only and differs from the actual system.

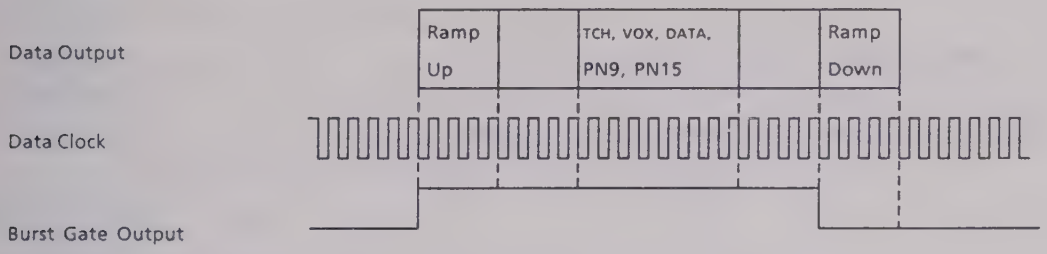


2.6.3 Burst gate signal

When the burst function is on and the internal pattern is used for modulation, a signal synchronized with the output slot in the frame is output..



The details about the slot are shown in the figure below. The format of the slot in this figure are for explanation purposes only and differs from the actual system.

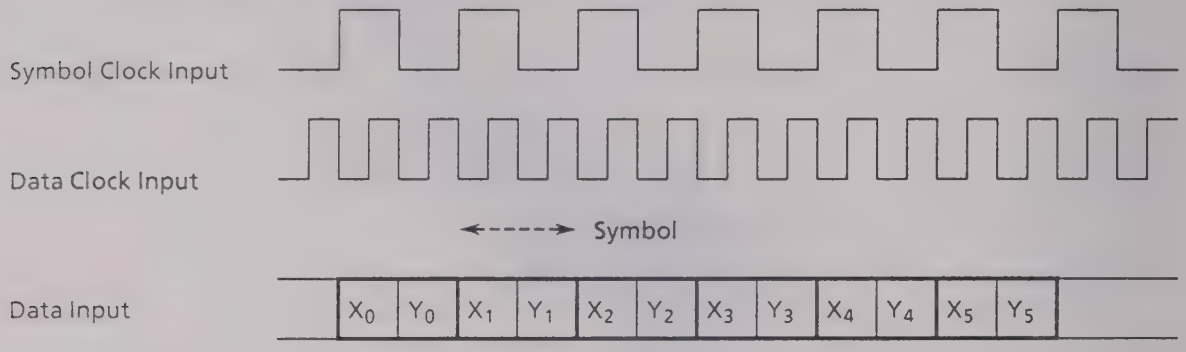


2.7 Auxiliary Inputs Signal

This paragraph explains the control signals input from the MG3670 series front panel.

2.7.1 Data, data clock and symbol clock signals

The input timings of the Data, Data Clock and Symbol Clock signals are shown below. In the figure, the polarities of the signals are expressed as positive or rising edge.



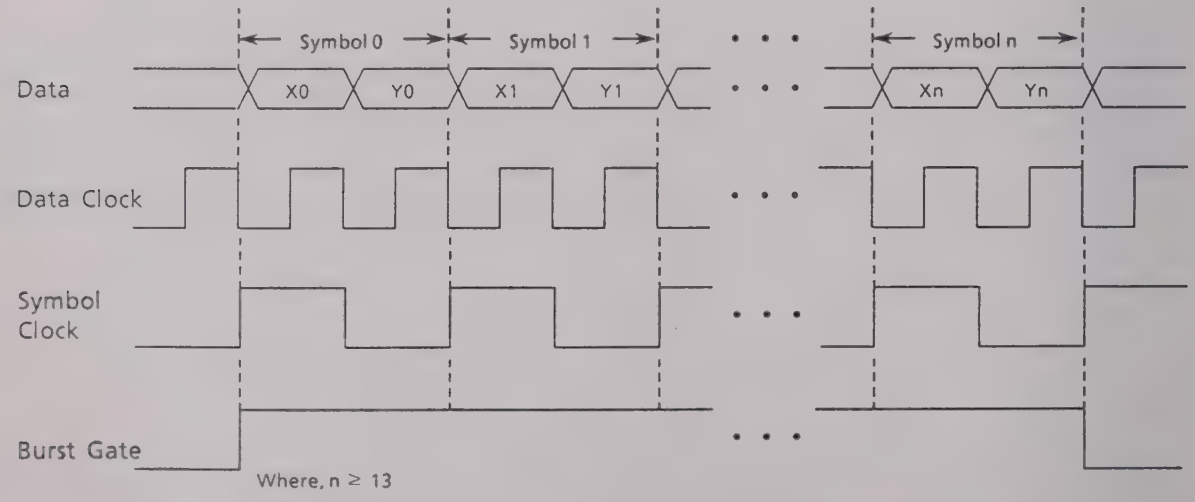
The symbol consists of Xn and Yn, where Xn indicates data that occurs before Yn.

Note: To input only one or two signals, synchronize the timing(s) with the output signal(s) of the signal(s) that will not be inputted.

2.7.2 Burst gate signal

When the burst function is On and data input is set to Ext, the burst gate signal can be fed externally. This signal can be fed in synchronously with the data signal timing in order to generate an RF burst signal identical to the burst signal generated from the internal pattern. (This will smoothen the slope of the rising and falling edges and prevent the spectrum from deteriorating.)

Shown below are the input timings of the Data, Data Clock, Symbol Clock and Burst Gate signals.



Note: The rising and falling edges of the power corresponds to Symbol 0, 1 and Symbol n+1, n+2, respectively.

2.8 Symbol Adjust Function

This function sets the symbol synchronization state in the case of $\pi/4$ DQPSK modulation.

■ Automatic synchronization function:

Function that synchronizes the internal symbol with the symbol clock input when in the symbol clock input mode.

Process: When the appropriate symbol clock is fed, the 'Symbol Adjust' F1 soft key disappears from the screen and the internal symbol is synchronized with the fed symbol clock.

■ Synchronization state select function:

Function that selects the symbol synchronization state when there is no symbol clock input in the symbol clock input mode.

Process: The symbol synchronization mode changes each time the 'Symbol Adjust' F1 soft key is pressed.

Shown below are the main instrument settings that can be used by the symbol adjust function.

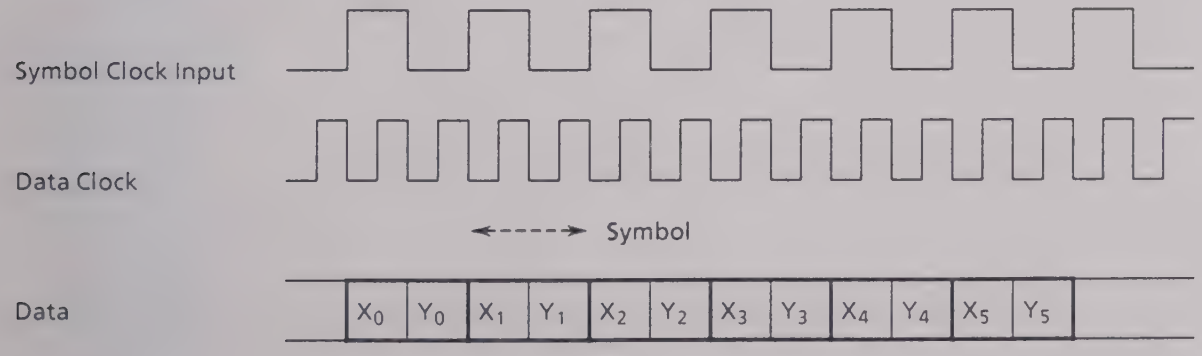
MG3670 series setting		Symbol Adjust function
Data Clock	Data	
Int	Int	Invalid
Int	Ext	Valid
Ext	Int	Valid
Ext	Ext	Valid

Invalid: Symbol clock cannot be input.

Valid: Synchronizes the symbol with the input symbol clock. When there is no input symbol clock, the symbol case, the Symbol Adjust key is used to select the symbol synchronization mode.

■ Inputting the symbol clock:

The input timing of the symbol clock is shown below. The polarities of all the signals are expressed as positive or rising edge.



The symbol consists of Xn and Yn, where Xn indicates data that occurs before Yn.

2.9 Phase Encode Function

This function inverts the direction of phase change against modulation data, changing the differential phase encoding specification at the π/4DQPSK modulation. With this function, the right and left of modulation spectrum can be inverted with the carrier frequency as the center. The differential phase encoding specifications are shown in the table below.

Differential phase encoding specifications at π/4DQPSK modulation

XY	Phase change $\Delta\Phi$ [rad]	
	Normal	Inverse
11	$-3\pi/4$	$3\pi/4$
01	$3\pi/4$	$-3\pi/4$
00	$\pi/4$	$-\pi/4$
10	$-\pi/4$	$\pi/4$

CAUTION: *X and Y represent symbols composed of 2 bits each. X advances to Y timewise.*

SECTION 3
DETAILED OPERATIONS

This section describes the operation, generated patterns and the trigger function of the MG0307A $\pi/4$ DQPSK Modulation Unit and the MG0303B Burst Function Unit for each system.

TABLE OF CONTENTS

3.1 Operating the PACS System 3-3
3.1.1 Frame composition 3-3
3.1.2 Slot composition 3-3
3.1.3 Standard internal modulation data 3-5

3.2 Operating the PHS System 3-7
3.2.1 Frame composition 3-7
3.2.2 Slot composition 3-7
3.2.3 Standard internal modulation data 3-11

3.3 Operating the WCPE System 3-14
3.3.1 Full Slot transmission 3-14
3.3.2 Double Slot transmission 3-23
3.3.3 Half Slot transmission 3-28

3.4 Detailed Trigger Function 3-33
3.4.1 Operation of the internal trigger 3-33
3.4.2 Operation of the external trigger 3-33
3.4.3 Output Timing of Burst Trigger and RF Signals 3-35
3.4.4 Relationships Between RF Signal and Symbol Judgment Point 3-38

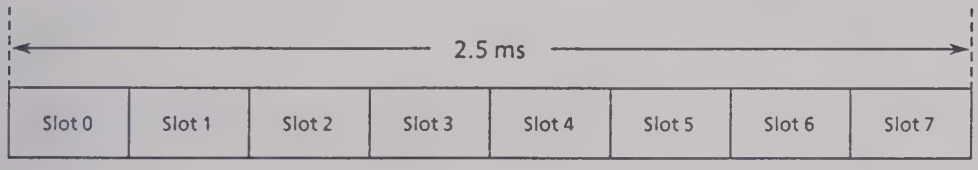
(Blank)

SECTION 3
DETAILED OPERATIONS

3.1 Operating the PACS System

3.1.1 Frame composition

The TDMA frame consists of eight slots. Signals are generated with one frame as one cycle. The PN9/PN15 pseudorandom pattern is independent for each slot and is continuous.



3.1.2 Slot composition

There are three types of slot for this system, namely, device evaluation slot, communication channel (uplink/downlink).

(1) Device evaluation slot (DEVICE)

G	PN
12	108

G : Guard time · · · 000_H (12 bits)
PN : Pseudorandom pattern · · · PN9-row pseudo-random pattern that has independence at each slot (PN pattern has continuity at the same slot.)

[Setting parameter]

- PN : PN9 or PN15 pseudorandom pattern

(2) Uplink communication channel (UP TCH)

G	DE	SC	FC	CRC	R
12	2	10	80	15	1

G : Guard time · · · 000_H (12 bits)
DE : Differential encode · · · 0_H (2 bits)
SC : Slow channel · · · 000_H (10 bits)
FC : Fast channel · · · PN9-row pseudo-random pattern that has independence at each slot (PN pattern has continuity at the same slot.)
CRC : Cyclic code bit (SC + FC) · · · Cyclic code bit for SC + FC (15 bits)
R : Reserved · · · 0_H (1 bit)

[Setting parameter]

- DE : $0_H \sim 3_H$ (2 bits)
- SC : $000_H \sim 3FF_H$ (10 bits)
- FC : PN9- or PN15-row pseudo-random pattern, and ALL "0" and ALL "1" (PN15-row pseudo-random pattern can be selected only for one slot.)
- R : $0_H \sim 1_H$ (1 bit)

(3) Downlink communication channel (DOWN TCH)

SYC	SC	FC	CRC	PCC
14	10	80	15	1

SYC : Synchronous bit · · · 0000_H (14 bits)
SC : Slow channel · · · 000_H (10 bits)
FC : Fast channel · · · PN9-row pseudo-random pattern that has independence at each slot (PN pattern has continuity at the same slot.)
CRC : Cyclic code bit (SC + FC) · · · Cyclic code bit for SC + FC (15 bits) (SLOT 7 is set to "7FFF".)
PCC : Power control channel · · · 0_H (1 bit) (SLOT 7 is set to "1")

[Setting parameter]

- SYC : $0000_H \sim 3FFF_H$ (14 bits)
- SC : $000_H \sim 3FF_H$ (10 bits)
- FC : PN9- or PN15-row pseudo-random pattern, and ALL "0" and ALL "1" (PN15-row pseudo-random pattern can be selected only for one slot.)
- PCC : $0_H \sim 1_H$ (1 bit)

3.1.3 Standard internal modulation data

There are five types of standard internal modulation data in the PACS system. To select the type of data, use 'Pattern' in the parameter setting screen (modulation parameter setting mode).

Note: • *'△' indicates the position of the burst trigger.*
• *All the slots 0 to 7 cannot be set to Off.*

(1) UP DEVICE

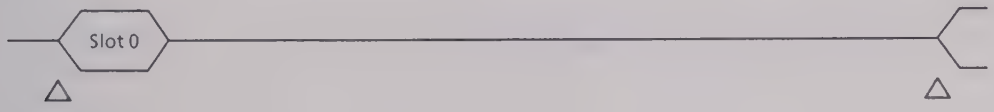
RF output using slot 0 as the device evaluation slot (DEVICE).

【 Setting parameter 】

- Slot: Slots 0 to 7 can be set to either DEVICE or OFF.

(2) UP TCH

RF output using slot 0 as the uplink communications channel (UP TCH).

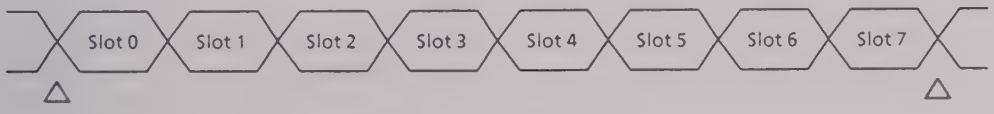


【 Setting parameter 】

- Slot: Slots 0 to 7 can be set to either UP TCH or OFF.

(3) UP TCH ALL

RF output using slots 0 to 7 as the uplink communications channels (UP TCH).

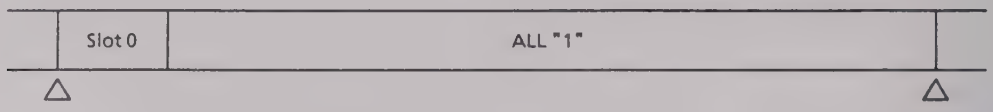


【 Setting parameter 】

- Slot: Slots 0 to 7 can be set to either UP TCH or OFF.

(4) DOWN TCH (DN TCH)

RF output using slot 0 as the downlink communications channel (DOWN TCH); The RF output is a continuous wave.

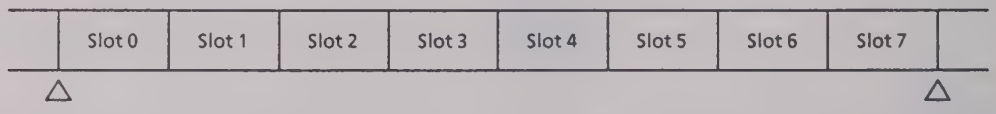


【 Setting parameter 】

- Slot: Slots 0 to 7 can be set to either DOWN TCH or OFF.
  (The output from an Off slot will consist of pure 1's.)

(5) DOWN TCH ALL (DN TCH ALL)

RF output using slots 0 to 7 as the downlink communications channels (DOWN TCH); The RF output is a continuous wave.



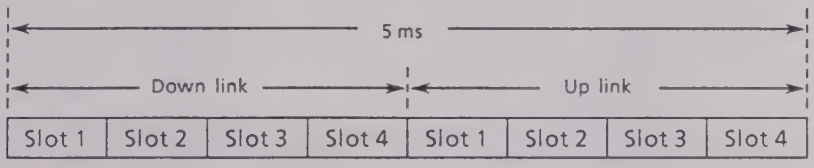
【 Setting parameter 】

- Slot: Slots 0 to 7 can be set to either DOWN TCH or OFF.
  (The output from an OFF slot will consist of pure 1's.)

3.2 Operating the PHS System

3.2.1 Frame composition

A TDMA frame consists of a total of 8 slots, four slot for the downlink and another four slot for the uplink. Signals are generated with one frame considered as one cycle. However, VOX control signals are generated with four frames equal to 20 ms. A slot output is produced for the first frame only, and no slot output is produced for the succeeding 2 to 4 frames. The PN9/PN15 pseudorandom pattern in the TCH of a slot is independent for each slot and is continuous.



3.2.2 Slot composition

There are four types of slots for this system, namely, device evaluation slot, TCH communication slot, VOX control slot and sync burst slot.

(1) Device evaluation (DEVICE)

R	PN	G
4	220	16

R: Ramp time · · · 0_H (4 bits)
PN: pseudorandom pattern · · · Independent PN9 pseudrordom pattern per slot (PN pattern in the same slot is continuous.)
G: Guard time · · · 0000_H (16 bits)
[Setting parameter]
•PN: PN9 or PN15 pseudorandom pattern

(2) Traffic channel (TCH)

R	SS	PR	UW	CI	SA	TCH	CRC	G
4	2	6	16	4	16	160	16	16

R: Ramp time · · · 0_H (4 bits)
SS: Start symbol · · · 2_H (2 bits)
RR: Preamble · · · 19_H (6 bits)
UW: Unique word · · · Uplink = $E149_H$ (16 bits)
Downlink = $3D4C_H$ (16 bits)
CI: Channel identifier · · · 0_H (4 bits)
SA: SACCH (Slow associated control channel) · · · 8000_H (16 bits)
TCH: Traffic channel · · · Independent PN9 pseudorandom pattern per slot (The PN pattern in the TCH field of the same slot is continuous.)
CRC: Cyclic redundancy check · · · CRC bits of CI, SA, and TCH
G: Guard time · · · 0000_H (16 bits)
Scramble function (TCH, CRC) · · · On
Scramble code · · · 200_H (10 bits)
Simple security function (TCH) · · · On
Password code · · · 0000_H (16 bits)

[Setting parameter]

- UW: 0000_H to $FFFF_H$ (16 bits)
- SA: 0000_H to $FFFF_H$ (16 bits)
- TCH: PN9 or PN15 pseudorandom pattern
- Scramble function: On / Off
- Scramble code: 000_H to $3FF_H$ (10bits)
- Simple security function: On / Off
- Password code: 0000_H to $FFFF_H$ (16bits)

(3) Voice operated transmission (VOX)

R	SS	PR	UW	CI	SA	VOX	CRC	G
4	2	6	16	4	16	160	16	16

R: Ramp time · · · 0_H (4 bits)
SS: Start symbol · · · 2_H (2 bits)
RR: Preamble · · · 19_H (6 bits)
UW: Unique word · · · Uplink = $E149_H$ (16 bits)
Downlink = $3D4C_H$ (16 bits)
CI: Channel identifier · · · F_H (4 bits)
SA: SACCH (Slow associated control channel) · · · 8000_H (16 bits)
TCH: Traffic channel · · · Independent PN9 pseudorandom pattern per slot (The PN pattern in the VOX field of the same slot is continuous.)
CRC: Cyclic redundancy check · · · CRC bits of CI, SA, and TCH
G: Guard time · · · 0000_H (16 bits)
Scramble function (TCH, CRC) · · · On
Scramble code · · · 200_H (10 bits)
Simple security function (TCH) · · · On
Password code · · · 0000_H (16 bits)

[Setting parameter]

- UW: 0000_H to $FFFF_H$ (16 bits)
- SA: 0000_H to $FFFF_H$ (16 bits)
- TCH: PN9 or PN15 pseudorandom pattern
- Scramble function: On / Off
- Scramble code: 000_H to $3FF_H$ (10 bits)
- Simple security function: On / Off
- Password code: 0000_H to $FFFF_H$ (16 bits)

(4) Sync burst (SYNC)

R	SS	PR	UW	CI	CS-ID	PS-ID	Idle	CRC	G
4	2	62	32	4	42	28	34	16	16

R: Ramp time · · · 0_H (4 bits)
SS: Start symbol · · · 2_H (2 bits)
RR: Preamble · · · 1999999999999999_H (62 bits)
UW: Unique word · · · Uplink = $68899AF0_H$ (32 bits)
Downlink = $50EF2993_H$ (32 bits)
CI: Channel identifier · · · 9_H (4 bits)
CS-ID: Cell station ID code · · · 20200020001_H (42 bits)
PS-ID: Personal station ID code · · · 0000001_H (28 bits)
Idle: Idle bit · · · 000000000_H (34 bits)
CRC: Cyclic redundancy check · · · CRC bits of CI, CS-ID, PS-ID, and Idle
G: Guard time · · · 0000_H (16 bits)
Scramble function (CS-ID, PS-ID, Idle, CRC) · · · On
Scramble code · · · 200_H (16 bits)
[Setting parameter]

- UW: $00000000_H \sim FFFFFFFF_H$ (32 bits)
- CI: $0_H \sim F_H$ (4 bits)
- CS-ID: $00000000000_H \sim 3FFFFFFFFFF_H$ (42 bits)
- PS-ID: $0000000_H \sim FFFFFFF_H$ (28 bits)
- Idle: $000000000_H \sim 3FFFFFFFF_H$ (34 bits)
- Scramble function: On / Off
- Scramble code: 000_H to $3FF_H$ (10 bits)

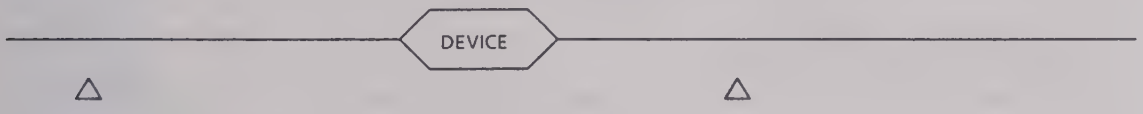
3.2.3 Standard internal modulation data

There are ten types of standard internal modulation data in the PHS system. To select the type of data, use 'Pattern' in the parameter setting screen (modulation parameter setting mode).

Note: • *'△' indicates the position of the burst trigger.*
• *All the slots 1 to 4 cannot be set to Off.*

(1) DEVICE

RF output using the uplink circuit slot 1 as the device evaluation slot

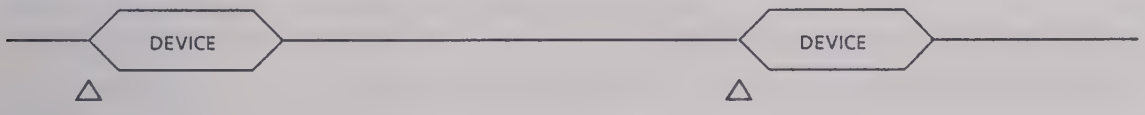


【 Setting parameter 】

• Slot: The uplink circuit slots 1 to 4 can be set to either DEVICE or OFF.

(2) DOWN DEVICE (DN DEVICE)

RF output using the downlink circuit slot 1 as the device evaluation slot



【 Setting parameter 】

• Slot: The downlink circuit slots 1 to 4 can be set to either DEVICE or OFF.

(3) UP TCH

RF output using the uplink circuit slot 1 as the TCH transmit slot

【 Setting parameter 】

• Slot: The uplink circuit slots 1 to 4 can be set to either TCH or OFF.

(4) UP TCH ALL

RF output using all the uplink circuits which include slots 1 to 4 as the TCH transmit slot

【 Setting parameter 】

- Slot: The uplink circuit slots 1 to 4 can be set to either UP TCH or OFF.

(5) DOWN TCH (DN TCH)

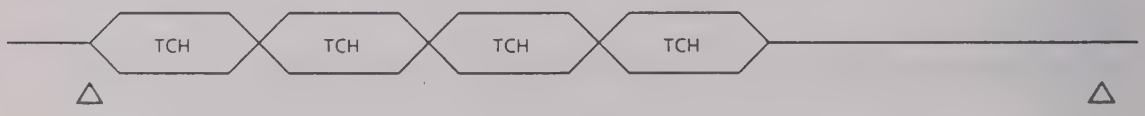
RF output using the downlink circuit slot 1 as the TCH transmit slot

【 Setting parameter 】

- Slot: The downlink circuit slots 1 to 4 can be set to DOWN TCH, VOX, or OFF.

(6) DOWN TCH ALL (DN TCH ALL)

RF output using all the downlink circuits which include slots 1 to 4 as the TCH transmit slot

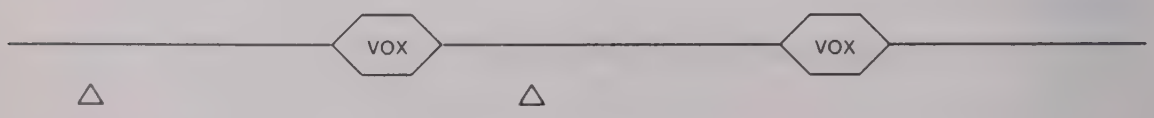


【 Setting parameter 】

- Slot: The downlink circuit slots 1 to 4 can be set to DOWN TCH, VOX, or OFF.

(7) UP VOX

RF output using the uplink circuit slot 1 as VOX control slot



【 Setting parameter 】

- Slot: The uplink circuit slots 1 to 4 can be set to either VOX or OFF.

Note: The VOX control slot is produced every four frames. The burst trigger is also generated once every 4 frames.

(8) DOWN VOX (DN VOX)

RF output using downlink slot 1 as the VOX control slot

【 Setting parameter 】

- Slot: Downlink slots 1 to 4 can be set to TCH, VOX or OFF.

(9) UP SYNC

RF output using uplink slot 1 as the sync burst slot

【 Setting parameter 】

- Slot: The uplink slots 1 to 4 can be set to either TCH or OFF.
  Either one of slots can be set to SYNC.

(10) DOWN SYNC (DN SYNC)

RF output using downlink slot 1 as the sync burst slot

【 Setting parameter 】

- Slot: The downlink slots 1 to 4 can be set to either TCH, VOX or OFF.
  Either one of slots can be set to SYNC.

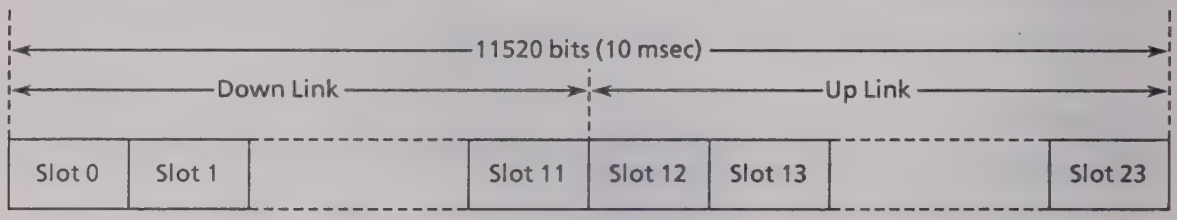
3.3 Operating the WCPE system

WCPE system has full slot transmission, double slot transmission and half slot transmission. These transmissions has each frame composition.

3.3.1 Full Slot transmission

3.3.1.1 Frame composition

A TDMA frame consists of 24 slots, slots 0 to 11 for the down link and slots 12 to 23 for the up link.



3.3.1.2 Slot composition

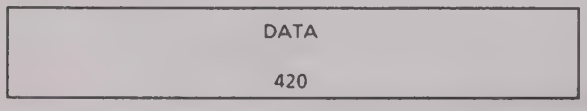
(1) Device evaluation slot (DEV P00)

DATA : User data transfer · · · Independent PN9 pseudorandom pattern per slot.
(The PN pattern in the DATA field of the same slot is continuous.)

[Setting parameter]

- DATA : PN9 or PN15 pseudorandom pattern, All "1" or All "0" pattern.

(2) Device evaluation slot (DEV P32)



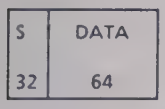
DATA : User data transfer · · · Independent PN9 pseudorandom pattern per slot.
(The PN pattern in the DATA field of the same slot is continuous.)

Z : Collision Detection · · · Off (fixed)

[Setting parameter]

- DATA : PN9 or PN15 pseudorandom pattern, All "1" or All "0" pattern.

(3) Device evaluation slot (DEV P00 S)



S : Synchronization word · · · $9999B1E4_H$ (32 bits) ; Down link
$66664E1B_H$ (32 bits) ; Up link

DATA : User data transfer · · · Independent PN9 pseudorandom pattern per slot.
(The PN pattern in the DATA field of the same slot is continuous.)

[Setting parameter]

- DATA : PN9 or PN15 pseudorandom pattern, All "1" or All "0" pattern.
- S : 00000000_H to $FFFFFFFF_H$ (32 bits)

(4) Device evaluation slot (DEV P32 S)

S : Synchronization word · · · $9999B1E4_H$ (32 bits) ; Down link
$66664E1B_H$ (32 bits) ; Up link

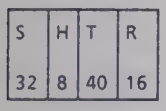
DATA : User data transfer · · · Independent PN9 pseudorandom pattern per slot.
(The PN pattern in the DATA field of the same slot is continuous.)

Z : Collision Detection · · · On

[Setting parameter]

- DATA : PN9 or PN15 pseudorandom pattern, All "1" or All "0" pattern.
- S : 00000000_H to $FFFFFFFF_H$ (32 bits)
- Z : On/Off

(5) Traffic channel (P00)



S : Synchronization word · · · $9999B1E4_H$ (32 bits) ; Down link
$66664E1B_H$ (32 bits) ; Up link

H : Header · · · CE_H (8 bits)

T : Tail · · · 21_H + PN9 pseudorandom pattern
(The PN pattern in the T field of the same slot is continuous.)

R : Cyclic redundancy check · · · CRC bits of H and T
When T field uses pseudorandom pattern, R is fixed "0000_H" pattern.
(Except following a case.)
When H field is CE_H and T field is 21_H + PN9, R is CRC bits.

[Setting parameter]

- S : 00000000_H to $FFFFFFFF_H$ (32 bits)
- H : 00_H to FF_H (8 bits)
- T : 00_H to FF_H (8 bits) + 00000000_H to $FFFFFFFF_H$ (32 bits)
or 00_H to FF_H (8 bits) + PN9/PN15 pseudorandom pattern

(6) Traffic channel (P32)

S	H	T	R	DATA	X	Z
32	8	40	16	320	4	4

S : Synchronization word · · · $9999B1E4_H$ (32 bits) ; Down link
$66664E1B_H$ (32 bits) ; Up link
H : Header · · · CE_H (8 bits)
T : Tail · · · $21_H + 0F0F0F0F_H$
R : Cyclic redundancy check · · · CRC bits of H and T
DATA : User data transfer · · · Independent PN9 pseudorandom pattern per slot.
(The PN pattern in the DATA field of the same slot is continuous.)
X : Cyclic redundancy check · · · CRC bits of DATA
Z : Collision Detection · · · On

[Setting parameter]

- S : 00000000_H to $FFFFFFFF_H$ (32 bits)
- H : 00_H to FF_H (8 bits)
- T : 00_H to FF_H (8 bits) + 00000000_H to $FFFFFFFF_H$ (32 bits)
- DATA : PN9, PN15, Test Pattern (TEST PATT) or Repetition Pattern (REP PATT)
- Z : On/Off

※ TEST PATT : DATA field are following pattern.
Where, b_0 to b_{319} means each bit of DATA field.

TEST PATT
- b_0 to b_{127}, b_{256} to b_{319} : "101010..."
- b_{128} to b_{191} : "1"
- b_{192} to b_{255} : "0"

REP PATT : DATA field are repetition of the 8 bits pattern (00_H to FF_H)

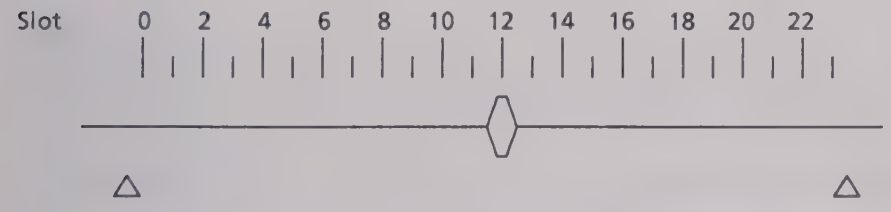
3.3.1.3 Standard internal modulation data

There are sixteen types of standard internal modulation data in the full slot transmission. To select the type of data, use "Pattern" in the parameter setting screen (modulation parameter setting mode).

Notes: • *"△" indicates the position of the burst trigger.*
• *All the slots cannot be set to Off.*

(1) UP DEVICE P00 (UP DEV P00)

RF output applying device evaluation slots (DEV P00) to slot 12.

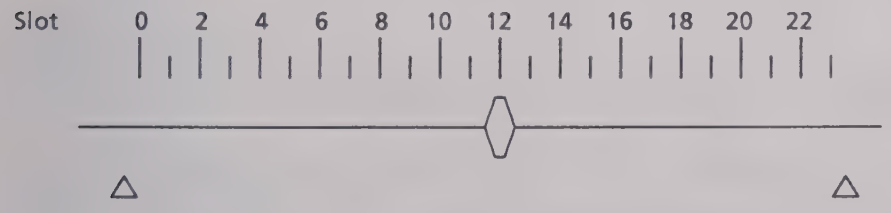


【 Setting parameter 】

Slot 12 to 23 can be set to DEV P00, DEV P00 S, DEV P32, DEV P32 S or Off.

(2) UP DEVICE P00 SYNC (UP DEV P00 S)

RF output applying device evaluation slots (DEV P00 S) to slot 12.

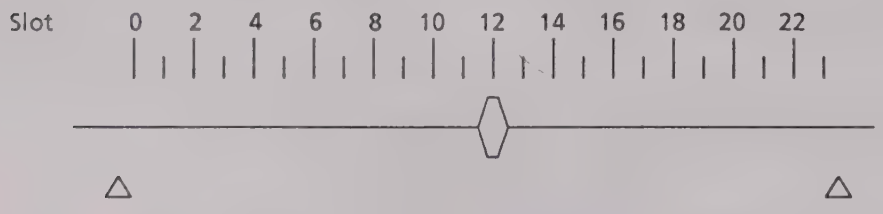


【 Setting parameter 】

Slot 12 to 23 can be set to DEV P00, DEV P00 S, DEV P32, DEV P32 S or Off.

(3) UP DEVICE P32 (UP DEV P32)

RF output applying device evaluation slots (DEV P32) to slot 12.

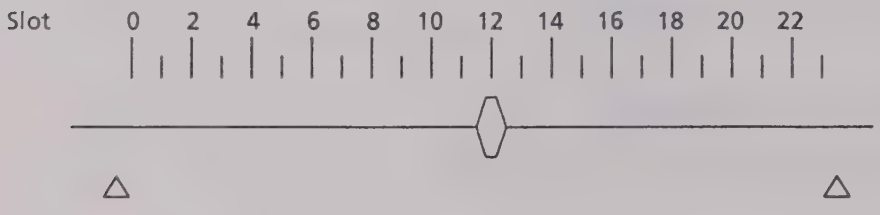


【 Setting parameter 】

Slot 12 to 23 can be set to DEV P00, DEV P00 S, DEV P32, DEV P32 S or Off.

(4) UP DEVICE P32 SYNC (UP DEV P32 S)

RF output applying device evaluation slots (DEV P32 S) to slot 12.

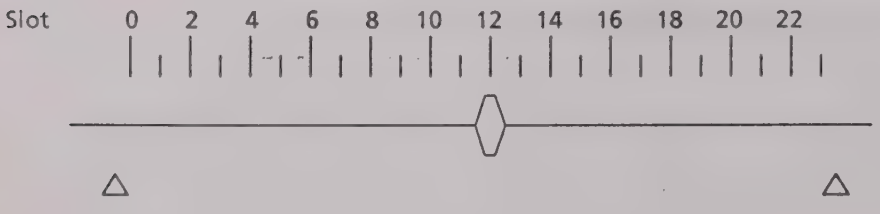


【 Setting parameter 】

Slot 12 to 23 can be set to DEV P00, DEV P00 S, DEV P32, DEV P32 S or Off.

(5) Up link traffic channel (UP P00)

RF output applying traffic channel slots (P00) to slot 12.

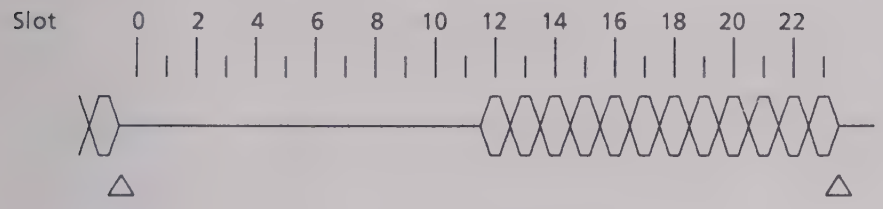


【 Setting parameter 】

Slot 12 to 23 can be set to P00, P32 or Off.

(6) Up link traffic channel (UP P00 ALL)

RF output applying traffic channel slots (P00) to slots 12 to 23.

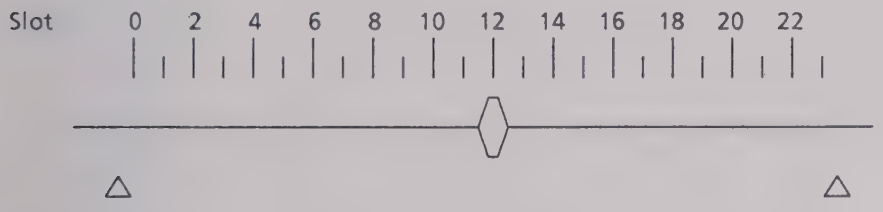


【 Setting parameter 】

Slot 12 to 23 can be set to P00, P32 or Off.

(7) Up link traffic channel (UP P32)

RF output applying traffic channel slots (P32) to slot 12.

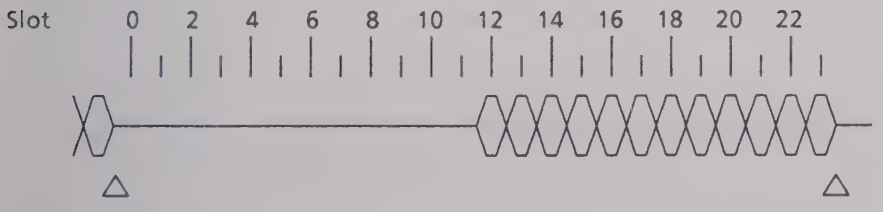


【 Setting parameter 】

Slot 12 to 23 can be set to P00, P32 or Off.

(8) Up link traffic channel (UP P32 ALL)

RF output applying traffic channel slots (P32) to slots 12 to 23.

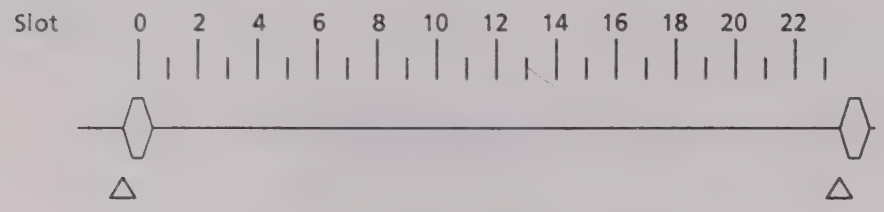


【 Setting parameter 】

Slot 12 to 23 can be set to P00, P32 or Off.

(9) DOWN DEVICE P00 (DN DEV P00)

RF output applying device evaluation slots (DEV P00) to slot 0.

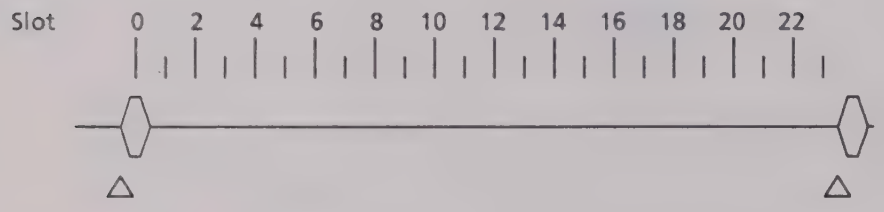


【 Setting parameter 】

Slot 0 to 11 can be set to DEV P00, DEV P00 S, DEV P32, DEV P32 S or Off.

(10) DOWN DEVICE P00 SYNC (DN DEV P00 S)

RF output applying device evaluation slots (DEV P00 S) to slot 0.

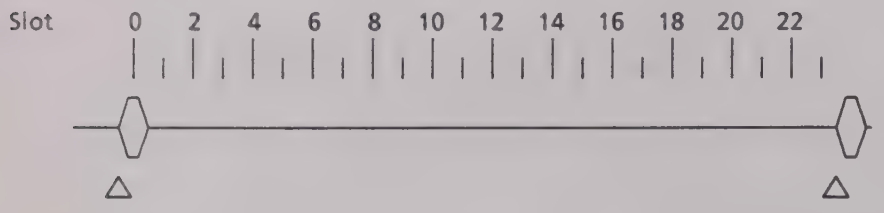


【 Setting parameter 】

Slot 0 to 11 can be set to DEV P00, DEV P00 S, DEV P32, DEV P32 S or Off.

(11) DOWN DEVICE P32 (DN DEV P32)

RF output applying device evaluation slots (DEV P32) to slot 0.

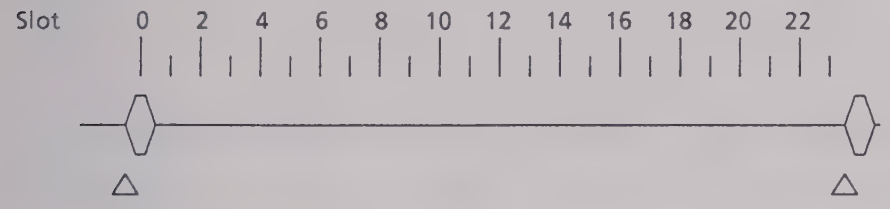


【 Setting parameter 】

Slot 0 to 11 can be set to DEV P00, DEV P00 S, DEV P32, DEV P32 S or Off.

(12) DOWN DEVICE P32 SYNC (DN DEV P32 S)

RF output applying device evaluation slots (DEV P32 S) to slot 0.

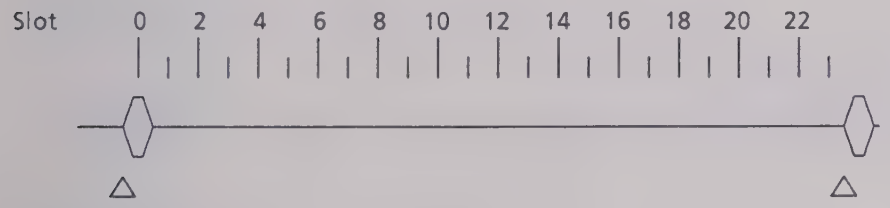


【 Setting parameter 】

Slot 0 to 11 can be set to DEV P00, DEV P00 S, DEV P32, DEV P32 S or Off.

(13) DOWN P00 (DN P00)

RF output applying traffic channel slots (P00) to slot 0.

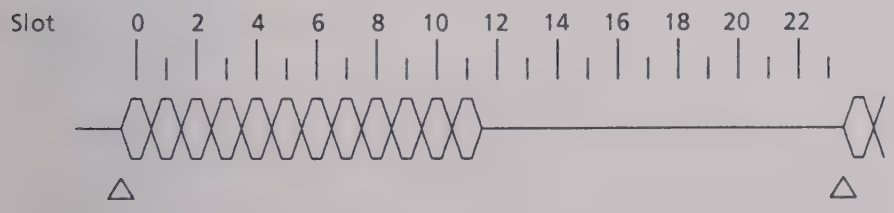


【 Setting parameter 】

Slot 0 to 11 can be set to P00, P32 or Off.

(14) DOWN P00 ALL (DN P00 ALL)

RF output applying traffic channel slots (P00) to slots 0 to 11.

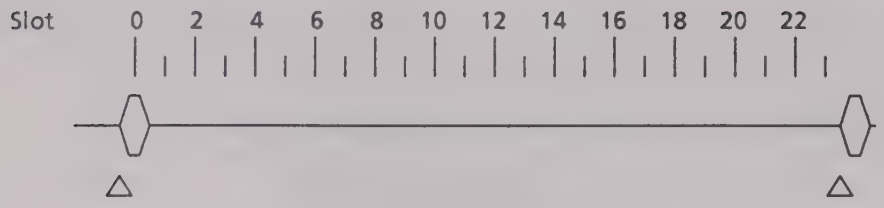


【 Setting parameter 】

Slot 0 to 11 can be set to P00, P32 or Off.

(15) DOWN P32 (DN P32)

RF output applying traffic channel slots (P32) to slot 0.

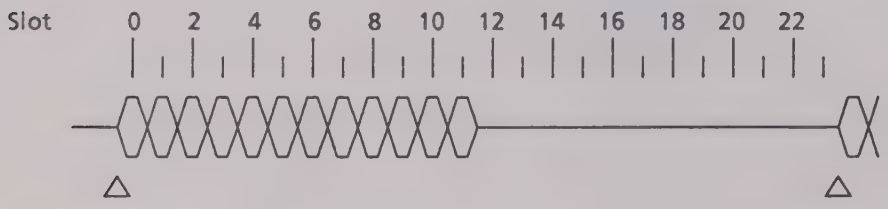


【 Setting parameter 】

Slot 0 to 11 can be set to P00, P32 or Off.

(16) DOWN P32 ALL (DN P32 ALL)

RF output applying traffic channel slots (P32) to slots 0 to 11.



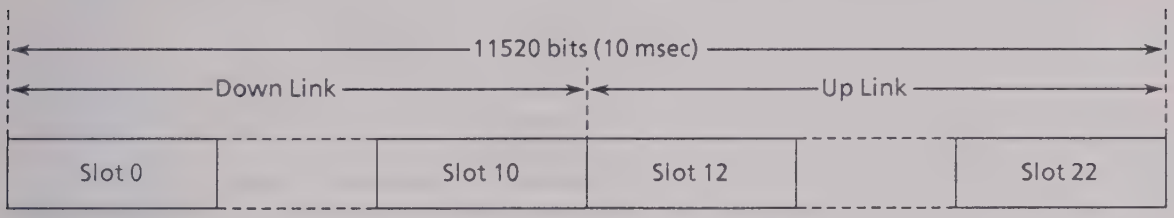
【 Setting parameter 】

Slot 0 to 11 can be set to P00, P32 or Off.

3.3.2 Double Slot transmission

3.3.2.1 Frame composition

A TDMA frame consists of 12 slots, slots 0 to 10 for the down link and slots 12 to 22 for the up link.



3.3.2.2 Slot composition

(1) Device evaluation slot (DEV P80)

DATA
900

DATA : User data transfer · · · Independent PN9 pseudorandom pattern per slot.
(The PN pattern in the DATA field of the same slot is continuous.)

[Setting parameter]

- DATA : PN9 or PN15 pseudorandom pattern, All "1" or All "0" pattern.

(2) Device evaluation slot (DEV P80 S)

S	DATA	Z
32	868	4

S : Synchronization word · · · $9999B1E4_H$ (32 bits) ; Down link
$66664E1B_H$ (32 bits) ; Up link

DATA : User data transfer · · · Independent PN9 pseudorandom pattern per slot.
(The PN pattern in the DATA field of the same slot is continuous.)

Z : Collision Detection · · · On

[Setting parameter]

- DATA : PN9 or PN15 pseudorandom pattern, All "1" or All "0" pattern.
- S : 00000000_H to $FFFFFFFF_H$ (32 bits)
- Z : On/Off

(3) Traffic channel (P80)

S	H	T	R	DATA	X	Z
32	8	40	16	800	4	4

S : Synchronization word · · · $9999B1E4_H$ (32 bits) ; Down link
$66664E1B_H$ (32 bits) ; Up link
H : Header · · · CE_H (8 bits)
T : Tail · · · $21_H + 0F0F0F0F_H$
R : Cyclic redundancy check · · · CRC bits of H and T
DATA : User data transfer · · · Independent PN9 pseudorandom pattern per slot.
(The PN pattern in the DATA field of the same slot is continuous.)
X : Cyclic redundancy check · · · CRC bits of DATA
Z : Collision Detection · · · On

[Setting parameter]

- S : 00000000_H to $FFFFFFFF_H$ (32 bits)
- H : 00_H to FF_H (8 bits)
- T : 00_H to FF_H (8 bits) + 00000000_H to $FFFFFFFF_H$ (32 bits)
- DATA : PN9, PN15, Test Pattern (TEST PATT) or Repetition Pattern (REP PATT)
- Z : On/Off

※ TEST PATT : DATA field are following pattern.
Where, b_0 to b_{799} means each bits of DATA field.

TEST PATT
- b_0 to b_{143}, b_{656} to b_{799} : "101010..."
- b_{144} to b_{655} : "1" 64 bits, "0" 64 bits , "1" 64 bits, "0" 64 bits , ···

REP PATT : DATA field are repetition of the 8 bits pattern (00_H to FF_H)

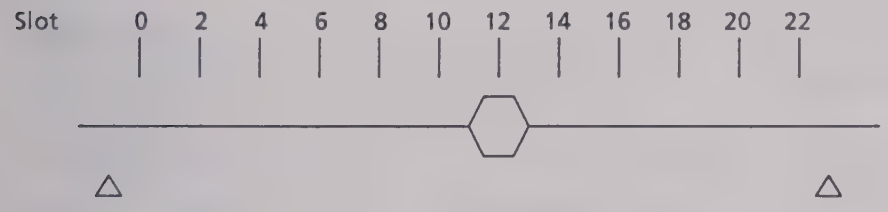
3.3.2.3 Standard internal modulation data

There are eight types of standard internal modulation data in the double slot transmission. To select the type of data, use "Pattern" in the parameter setting screen (modulation parameter setting mode).

Notes: • *"△" indicates the position of the burst trigger.*
• *All the slots cannot be set to Off.*

(1) UP DEVICE P80 (UP DEV P80)

RF output applying device evaluation slots (DEV P80) to slot 12.

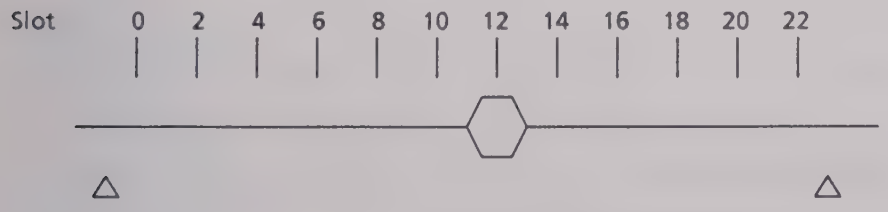


【 Setting parameter 】

Slot 12 to 22 can be set to DEV P80, DEV P80 S or Off.

(2) UP DEVICE P80 SYNC (UP DEV P80 S)

RF output applying device evaluation slots (DEV P80 S) to slot 12.

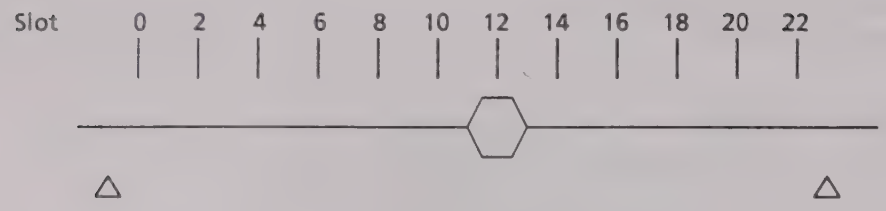


【 Setting parameter 】

Slot 12 to 22 can be set to DEV P80, DEV P80 S or Off.

(3) Up link traffic channel (UP P80)

RF output applying traffic channel slots (P80) to slot 12.

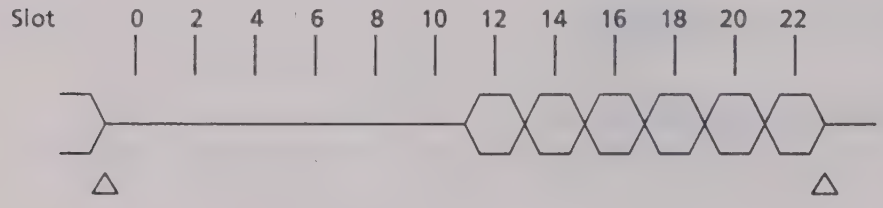


【 Setting parameter 】

Slot 12 to 22 can be set to P80 or Off.

(4) Up link traffic channel (UP P80 ALL)

RF output applying traffic channel slots (P80) to slots 12 to 22.

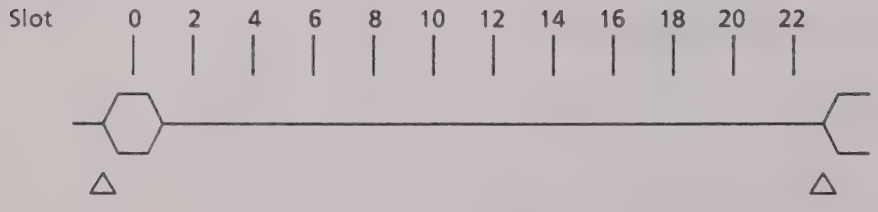


【 Setting parameter 】

Slot 12 to 22 can be set to P80 or Off.

(5) DOWN DEVICE P80 (DN DEV P80)

RF output applying device evaluation slots (DEV P80) to slot 0.

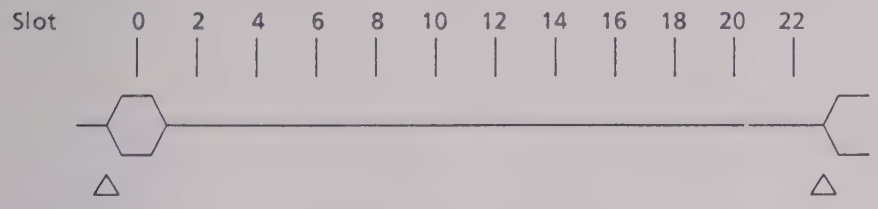


【 Setting parameter 】

Slot 0 to 10 can be set to DEV P80, DEV P80 S or Off.

(6) DOWN DEVICE P80 SYNC (DN DEV P80 S)

RF output applying device evaluation slots (DEV P80 S) to slot 0.

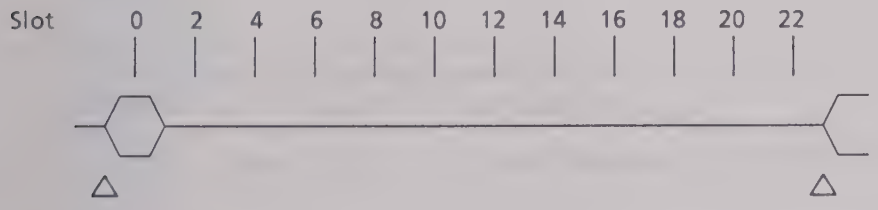


【 Setting parameter 】

Slot 0 to 10 can be set to DEV P80, DEV P80 S or Off.

(7) DOWN P80 (DN P80)

RF output applying traffic channel slots (P80) to slot 0.

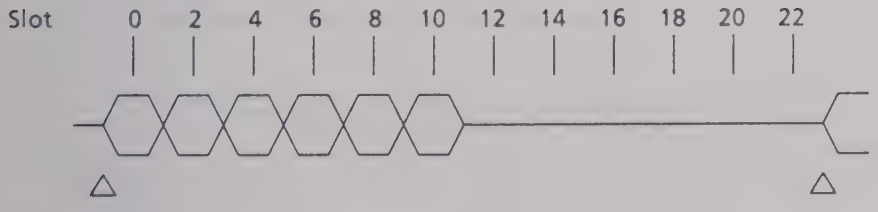


【 Setting parameter 】

Slot 0 to 10 can be set to P80 or Off.

(8) DOWN P80 ALL (DN P80 ALL)

RF output applying traffic channel slots (P80) to slots 0 to 10.



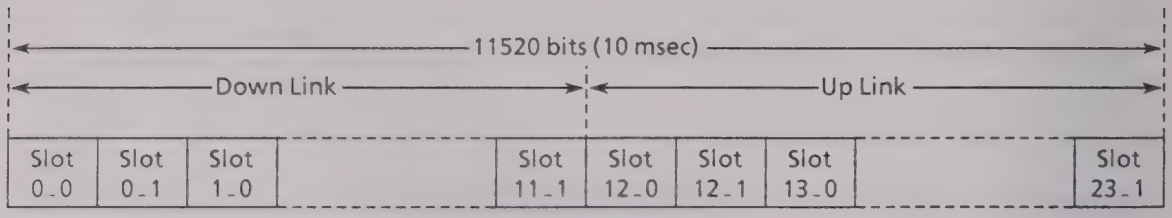
【 Setting parameter 】

Slot 0 to 10 can be set to P80 or Off.

3.3.3 Half Slot transmission

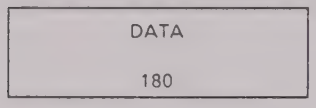
3.3.3.1 Frame composition

A TDMA frame consists of 48 slots, slots 0_0 to 11_1 for the down link and slots 12_0 to 23_1 for the up link.



3.3.3.2 Slot composition

(1) Device evaluation slot (DEV P08)



DATA : User data transfer · · · Independent PN9 pseudorandom pattern per slot.
(The PN pattern in the DATA field of the same slot is continuous.)

[Setting parameter]

- DATA : PN9 or PN15 pseudorandom pattern, All "1" or All "0" pattern.

(2) Device evaluation slot (DEV P08 S)

S : Synchronization word · · · $9999B1E4_H$ (32 bits) ; Down link
$66664E18_H$ (32 bits) ; Up link

DATA : User data transfer · · · Independent PN9 pseudorandom pattern per slot.
(The PN pattern in the DATA field of the same slot is continuous.)

Z : Collision Detection · · · On

[Setting parameter]

- DATA : PN9 or PN15 pseudorandom pattern, All "1" or All "0" pattern.
- S : 00000000_H to $FFFFFFFF_H$ (32 bits)
- Z : On/Off

(3) Traffic channel (P08)

S	H	T	R	DATA	X	Z
32	8	40	16	80	4	4

S : Synchronization word · · · $9999B1E4_H$ (32 bits) ; Down link
$66664E1B_H$ (32 bits) ; Up link

H : Header · · · CE_H (8 bits)

T : Tail · · · $21_H + 0F0F0F0F_H$

R : Cyclic redundancy check · · · CRC bits of H and T

DATA : User data transfer · · · Independent PN9 pseudorandom pattern per slot.
(The PN pattern in the DATA field of the same slot is continuous.)

X : Cyclic redundancy check · · · CRC bits of DATA

Z : Collision Detection · · · On

[Setting parameter]

- S : 00000000_H to $FFFFFFFF_H$ (32 bits)
- H : 00_H to FF_H (8 bits)
- T : 00_H to FF_H (8 bits) + 00000000_H to $FFFFFFFF_H$ (32 bits)
- DATA : PN9, PN15, Test Pattern (TEST PATT) or Repetition Pattern (REP PATT)
- Z : On/Off

※ TEST PATT : DATA field are following pattern.
TEST PATT = "$AAFF\ FFFF\ FF00\ 0000\ 00AA_H$"
REP PATT : DATA field are repetition of the 8 bits pattern (00_H to FF_H).

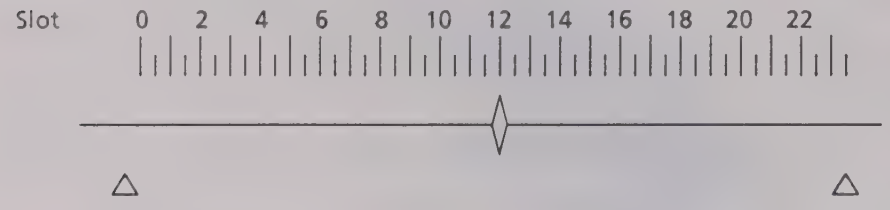
3.3.3.3 Standard internal modulation data

There are eight types of standard internal modulation data in the half slot transmission. To select the type of data, use "Pattern" in the parameter setting screen (modulation parameter setting mode).

Notes: • *"△" indicates the position of the burst trigger.*
• *All the slots cannot be set to Off.*

(1) UP DEVICE P08 (UP DEV P08)

RF output applying device evaluation slots (DEV P08) to slot 12_0.



【 Setting parameter 】

Slot 12_0 to 23_1 can be set to DEV P08, DEV P08 S or Off.

(2) UP DEVICE P08 SYNC (UP DEV P08 S)

RF output applying device evaluation slots (DEV P08 S) to slot 12_0.

【 Setting parameter 】

Slot 12_0 to 23_1 can be set to DEV P08, DEV P08 S or Off.

(3) Up link traffic channel (UP P08)

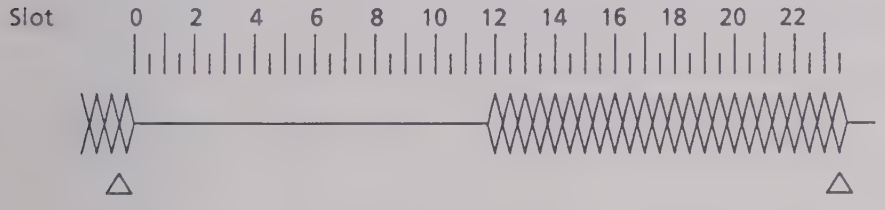
RF output applying traffic channel slots (P08) to slot 12_0.

【 Setting parameter 】

Slot 12_0 to 23_1 can be set to P08 or Off.

(4) Up link traffic channel (UP P08 ALL)

RF output applying traffic channel slots (P08) to slots 12_0 to 23_1.

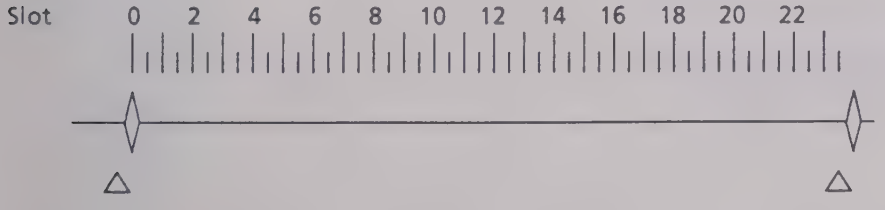


【 Setting parameter 】

Slot 12_0 to 23_1 can be set to P08 or Off.

(5) DOWN DEVICE P80 (DN DEV P08)

RF output applying device evaluation slots (DEV P08) to slot 0_0.

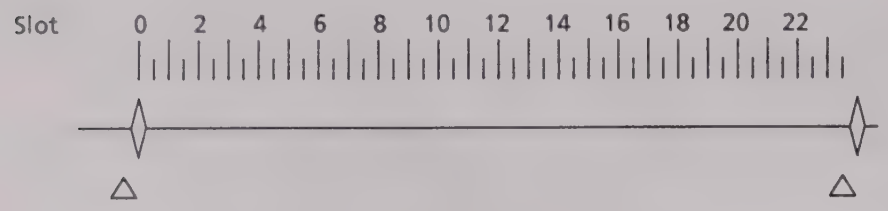


【 Setting parameter 】

Slot 0_0 to 11_1 can be set to DEV P08, DEV P08 S or Off.

(6) DOWN DEVICE P80 SYNC (DN DEV P08 S)

RF output applying device evaluation slots (DEV P08 S) to slot 0_0.

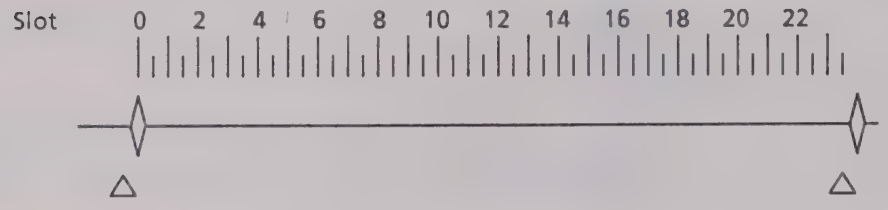


【 Setting parameter 】

Slot 0_0 to 11_1 can be set to DEV P08, DEV P08 S or Off.

(7) DOWN P08 (DN P08)

RF output applying traffic channel slots (P08) to slot 0_0.

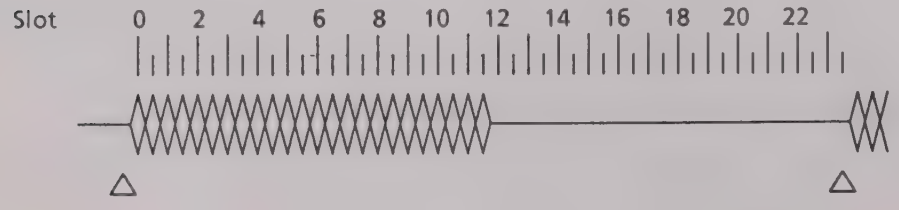


【 Setting parameter 】

Slot 0_0 to 11_1 can be set to P08 or Off.

(8) DOWN P08 ALL (DN P08 ALL)

RF output applying traffic channel slots (P08) to slots 0_0 to 11_1.



【 Setting parameter 】

Slot 0_0 to 11_1 can be set to P08 or Off.

3.4 Detailed Trigger Function

There are two trigger functions for generating burst signals when the burst function is on. These are:

① Internal trigger that works synchronously with the internal trigger signal
② External trigger that works synchronously with the external trigger signal.

3.4.1 Operation of the internal trigger

An internal trigger works by generating a burst signal synchronous with the internal trigger signal. This trigger signal is output from the Burst Trig Output connector on the rear panel. Since the trigger signal is produced at every cycle of the burst signal, its period can be fixed in every system.

3.4.2 Operation of the external trigger

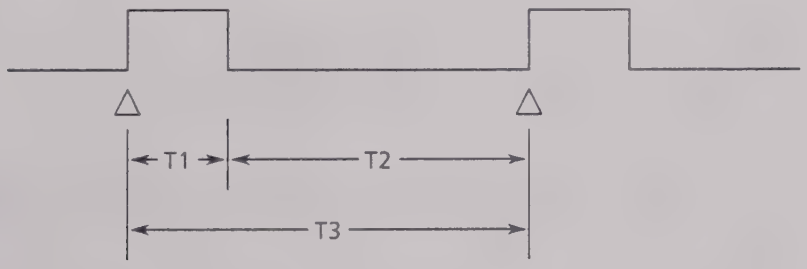
An external trigger works by generating a burst signal synchronous with the external fed trigger signal. This trigger signal is fed to the Burst Trig Input connector on the rear panel.

(1) External trigger signal input conditions

(a) Input level: TTL level

(b) Polarity : Either rising or falling edge can be selected

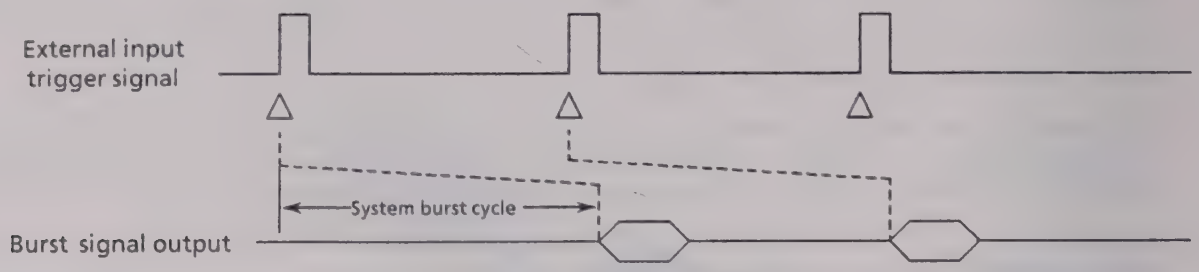
(c) Waveform : The waveform below illustrates a rising edge trigger waveform



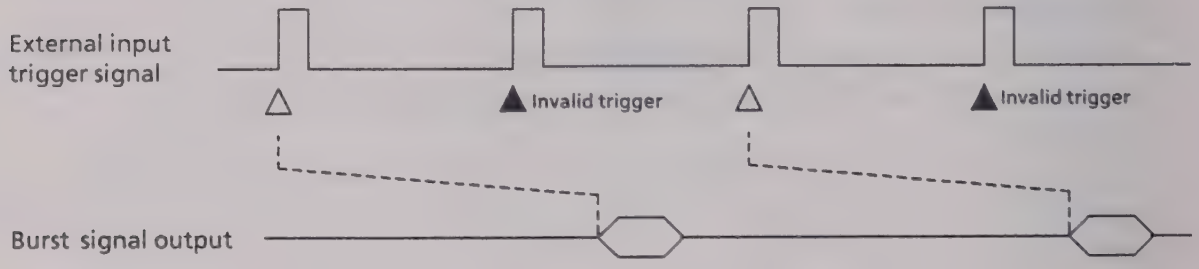
T1 : ≧0.1 μs
T2 : ≧0.1 μs
T3 : burst cycle (frame cycle) ± 1 symbol
Rising/falling time: 50 ns or less

(2) Relationship between external input trigger signal and output burst signal

The figure below illustrates that the external input trigger signal is produced after a delay of one burst cycle.



Note: *If the period of the external input trigger signal does not satisfy the input condition in (1), the trigger signal is masked and invalidated as illustrated in the figure below. Therefore, the burst signal synchronized with the trigger signal cannot be obtained.*

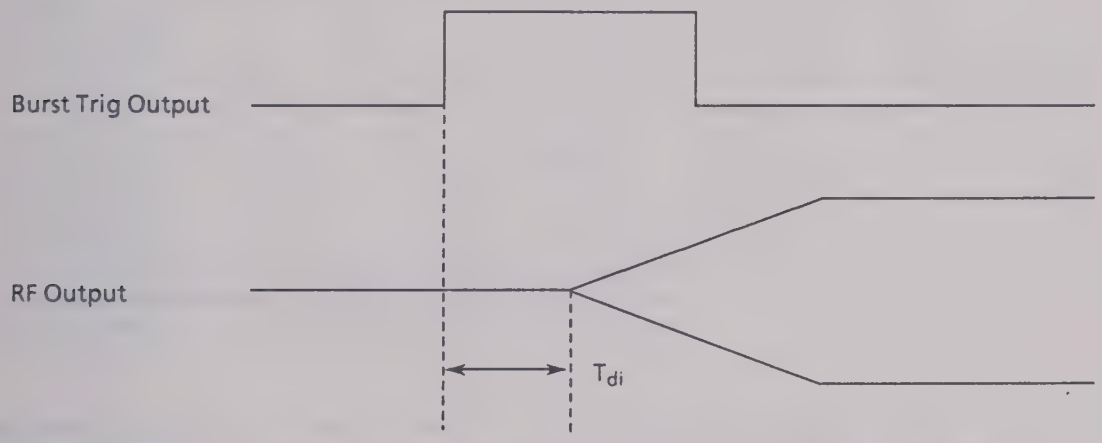


3.4.3 Output Timing of Burst Trigger and RF Signals

Pay attention to output timings of trigger and RF signals when synchronized with another equipment using the burst trigger signal of the MG3670 series. Relationships between trigger and RF signals are explained below.

(1) When internal trigger signal is used

The output timing of RF signal is shown below when synchronized with another equipment using the Burst TrigOutput signal from the MG3670 series rear panel.



T_{di}: Represents the delay time when burst wave is output using the internal trigger signal, which corresponds to the time from trigger until the start up of the first slot in the frame.

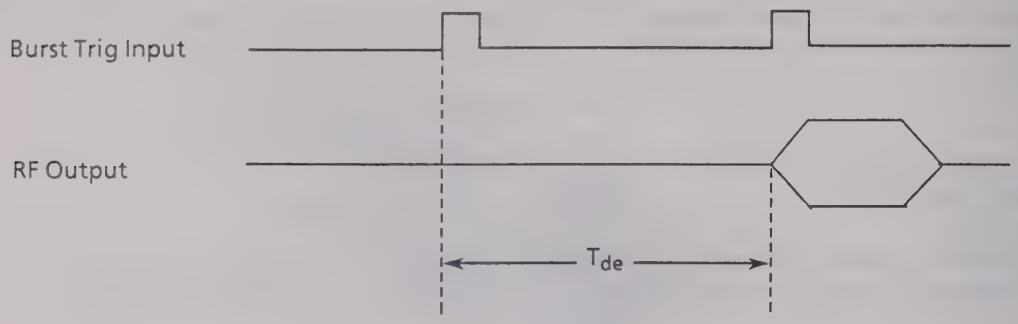
Relationships between communication system and T_{di}

Communication system	Delay time T_{di} ( ) indicates symbol converted value.
PACS	3.44 μs $\pm$ 0.10 μs (0.660 $\pm$ 0.019 symbol)
PHS	3.44 μs $\pm$ 0.10 μs (0.660 $\pm$ 0.019 symbol)
WCPE	0.62 μs $\pm$ 0.08 μs (0.357 $\pm$ 0.046 symbol)

CAUTION: *T_{di} includes error from system to system and is unique to each system, excluding the jitter.*

(2) When external trigger signal is used

The output timing of RF signal is shown below when synchronized with another equipment using the Burst TrigIntput signal to the MG3670 series rear panel. The RF signal is output with a delay equivalent to approximately 1 frame period (T_{de}) of the communication system from the trigger signal. This matches the timing of the second trigger signal to that of the RF output when a trigger signal meeting the communication system is input.



T_{de}: Represents the delay time when burst wave is output using the external trigger signal, which corresponds to the time from trigger until the start up of the first slot in the frame.

When an external trigger signal is used, the Tde value varies according to the mean used for synchronizing the MG3670 series with the trigger signal source equipment. The following explains T_{de} values by synchronization methods.

(A) When connecting only with trigger signal

The delay time is calculated using the formula below when only the trigger signal is input to the MG3670 series:

T_{de1} = Frame period of communication system + T_{di} + Synchronization error
(−0.47 ~ +0.54 symbol)

T_{de1}: Delay time for connection only by trigger signal
T_{di}: Delay time for operation with internal trigger signal
Synchronization error: Jitter occurs within −0.47 ~ +0.54 symbol since the MG3670 series is not synchronized with the external trigger signal source.

CAUTION: When the MG3670 series is synchronized with the external trigger signal source using the 10/13 MHz reference signal, no jitter occurs. The jitter value is inconsistent within a range the synchronization error.

Relationships between communication system and T_{de1}

Communication system	Delay time T_{de1} ( ) indicates symbol converted value.
PACS	2.5 ms + 3.44 μs + (−2.55 ~ +2.91) μs (1 frame + 0.660 symbol + (−0.489 ~ +0.559) symbol)
PHS	5 ms + 3.44 μs + (−2.55 ~ +2.91) μs (1 frame + 0.660 symbol + (−0.489 ~ +0.559) symbol)
WCPE	10 ms + 0.62 μs + (−0.89 ~ +1.02) μs (1 frame + 0.357 symbol + (−0.516 ~ +0.586) symbol)

(B) When Data Clock and Symbol Clock are connected

Delay times are calculated using the formula below when trigger signal is input to the MG3670 series with Data Clock and Symbol Clock connected:

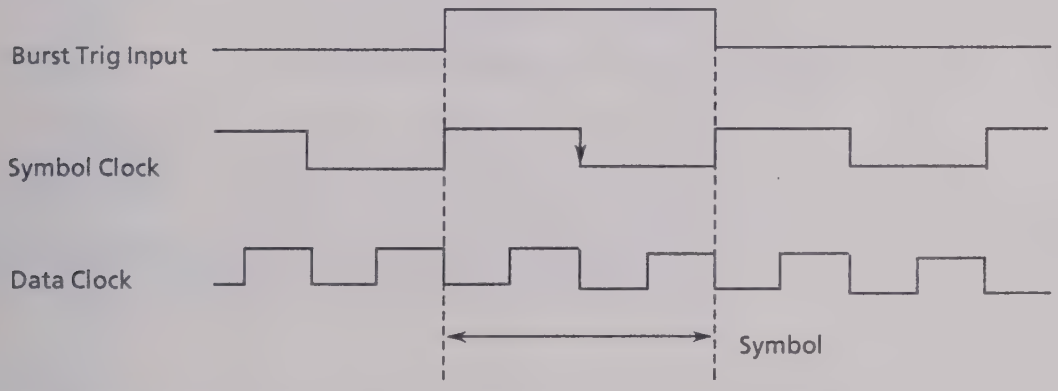
T_{de2} = (Frame period of communication system) + T_{di}

T_{de2}: Delay time when trigger signal, Data Clock and Symbol Clock are connected
T_{di}: Delay time when operated using the internal trigger signal

Relationships between communication system and T_{de2}

Communication system	Delay time T_{de2} ( ) indicates symbol converted value.
PACS	2.5 ms + (3.44 ± 0.10) μs (1 frame + (0.660 ± 0.019) symbol)
PHS	5 ms + (3.44 ± 0.10) μs (1 frame + (0.660 ± 0.019) symbol)
WCPE	10 ms + (0.62 ± 0.08) μs (1 frame + (0.357 ± 0.046) symbol)

The figure below shows timings of Data Clock, Symbol Clock and trigger signals. (When polarities of all signals are positive)



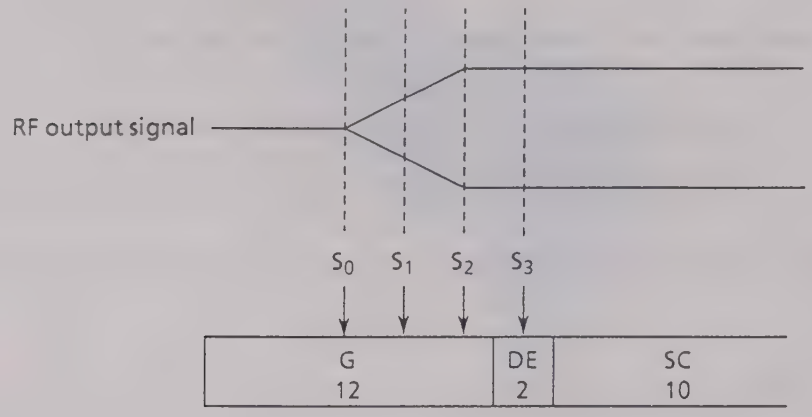
CAUTION: *Although it is possible to operate without inputting the Symbol Clock, phase relationships between the Symbol Clock and trigger signals will be undefined. In this case, adjust the phase relationships between the MG3670 series and Symbol Clock of the trigger signal source as shown above using the Symbol Adjust key. When Data Clock is used for synchronization, the trigger signal input timing is adjusted in 1 symbol steps since the Symbol Clock monitors the Burst Trig Input signal.*

3.4.4 Relationships Between RF Signal and Symbol Judgment Point

Relationships between the RF output signal and symbol judgment point vary according to the communication system. The relationships are, therefore, explained for each system. Here, the symbol judgment point is defined as the point where the impulse response of the base band filter is the maximum.

(1) PACS system

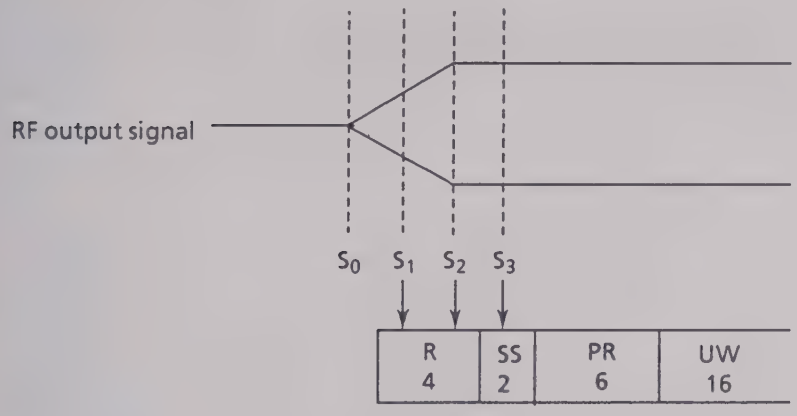
Relationships between modulation data against the RF signal and the symbol judgment point is explained using slot 0 of the uplink traffic channel as an example.



S_0 : Symbol generated by the 7th and 8th bits of the gard time
S_1 : Symbol generated by the 9th and 10th bits of the gard time
S_2 : Symbol generated by the 11th and 12th bits of the gard time
S_3 : Symbol generated by differential encode
The delay time from burst trigger signal to start up of RF output is the same as that from burst trigger signal to S_0.
(For details on delay time, refer to Paragraph 3.4.3.)

(2) PHS system

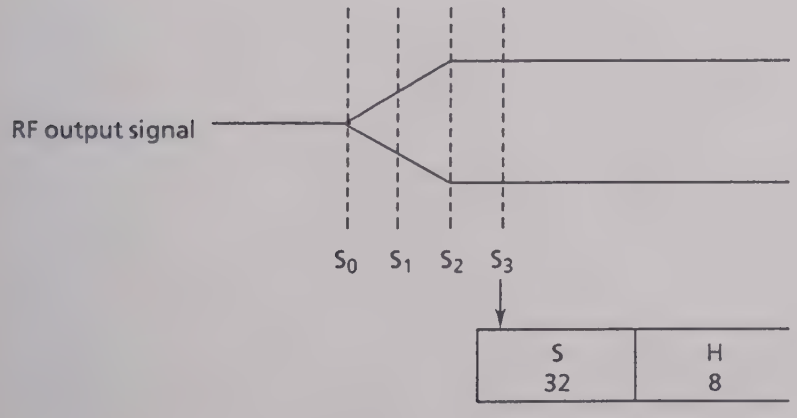
Relationships between modulation data against the RF signal and the symbol judgment point is explained using slot 1 of the downlink traffic channel as an example.



S_1: First symbol generated by the burst transient response ramp bit
S_2: Second symbol generated by the burst transient response ramp bit
S_3: Symbol generated by the start symbol
The delay time from burst trigger signal to start up of RF output is the same as that from burst trigger signal to S_0.
(For details on delay time, refer to Paragraph 3.4.3.)

(3) WCPE system

Relationships between modulation data against the RF signal and the symbol judgment point is explained using slot 0 of the traffic channel (P32) as an example.



S_3: First symbol generated by the sync word
The delay time from burst trigger signal to start up of RF output is the same as that from burst trigger signal to S0.
(For details on delay time, refer to Paragraph 3.4.3.)

(Blank)

SECTION 4
MEASUREMENT

This section describes how to perform code error rate measurement for receivers, demodulator evaluation measurement, and modulator evaluation measurement using the MG0307A $\pi/4$ DQPSK Modulation Unit and the MG0303B Burst Function Unit in combination with the MG3670 series Digital Modulation Signal Generator.

TABLE OF CONTENTS

4.1 Code Error Rate Measurement for Receiver 4-3

4.2 Demodulator Evaluation Measurement 4-5

4.3 Modulator Evaluation Measurement 4-6

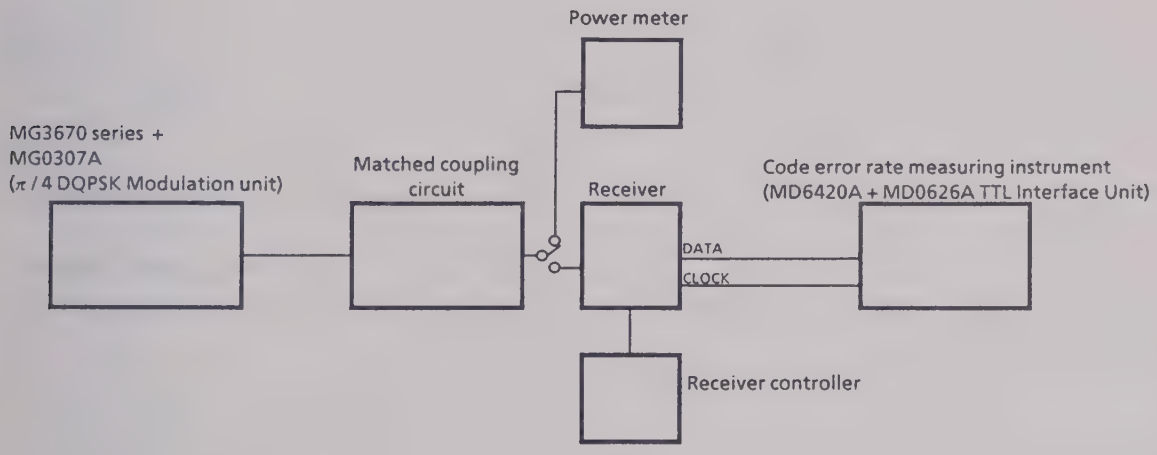
(Blank)

SECTION 4
MEASUREMENT

4.1 Code Error Rate Measurement for Receiver

The procedure for measuring a receiver code error rate using the MG3670 series + MG0307A system is described below. It is assumed that the receiver is equipped with a control mode that enables it to receive continuous waves.

(1) Setup



(2) Measurement procedure

Step	Procedure
1	Set the MG3670 series to the frequency to be tested.
2	Set the MG3670 series output to a level suitable for the receiver and the Matched coupling circuit.
3	Set the MG3670 series to the modulation system of the receiver.
4	Set the MG3670 series modulation pattern to PN9 pseudorandom pattern.
5	Connect the MG3670 series RF output to the power meter through the Matched coupling circuit. Using the power meter, adjust the MG3670 series output to the sensitivity test level.
6	Switch the Matched coupling circuit output to the receiver.
7	Using the receiver controller, set the receiver to the continuous wave reception mode.
8	Connect the receiver demodulation data output and data clock to the code error rate measuring instrument. The procedure when the code error rate measuring instrument used is Anritsu's MD6420A Data Transmission Analyzer is described below.
9	Connect the data and clock obtained from the receiver to the RD (Data) and RT (Clock) connectors of the TTL Interface Unit (MD0626A) on the rear panel of the MD6420A.

Step	Procedure
10	Set the MD6420A receive timing as follows: • If data is sampled at the rising edge of the clock, set to RT (INV) mode. • If data is sampled at the falling edge of the clock, set to RT mode.
11	Set the MD6420A pattern to 2^9-1 (PN9).
12	Press the MD6420A MEAS key to measure the code error rate.

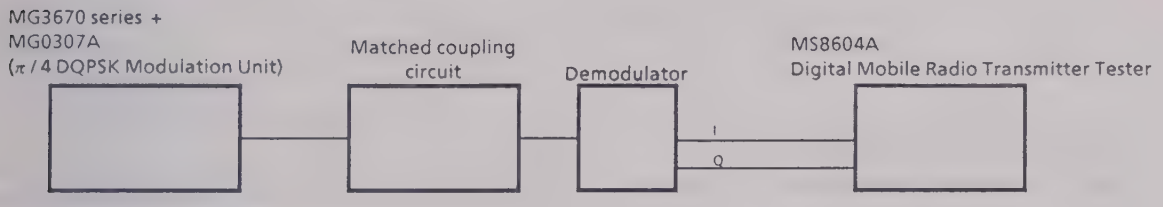
4.2 Demodulator Evaluation Measurement

The procedure for performing the evaluation measurement for a demodulator using the MG3670 series + MG0307A system is described below.

It is assumed that Anritsu's MS8604A Digital Mobile Radio Transmitter Tester is used in evaluating the demodulator I/Q signal output. Please note that the MS8604A requires the I-Q input function (option 03).

If the MG0303B Burst Function Unit is incorporated in the MG3670 series, it is also possible to perform evaluation using burst signals.

(1) Setup



(2) Measurement procedure

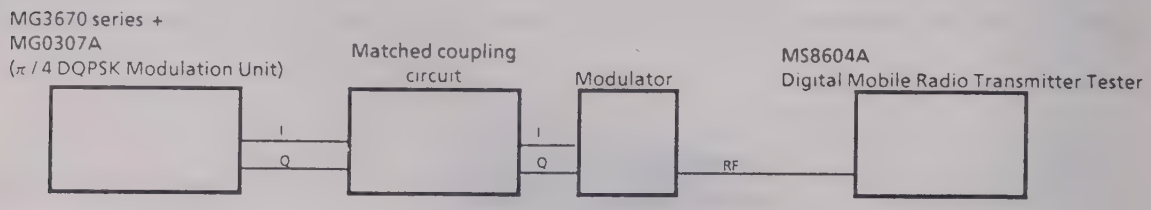
Step	Procedure
1	Set the MG3670 series to the frequency to be tested.
2	Set the MG3670 series output to a level suitable for the demodulator and the Matched coupling circuit.
3	Set the MG3670 series to the modulation system to be tested.
4	Set the MG3670 series modulation pattern to PN9 pseudorandom pattern. (If the MG0303B is incorporated, burst signal can also be set.)
5	Set the MS8604A so that the modulation system and pattern set in steps 3 and 4 can be received.
6	Using the MS8604A, measure the modulation accuracy and evaluate it. (For information on the MS8604A operation, refer to the MS8604A Operation Manual.)

4.3 Modulator Evaluation Measurement

The procedure for performing evaluation measurement for a modulator using the MG3670 series + MG0307A system is described below.

It is assumed that Anritsu's MS8604A Digital Mobile Radio Transmitter Tester is used in evaluating the modulator modulation signal output.

(1) Setup



(2) Measurement procedure

Step	Procedure
1	Set the MG3670 series I, Q signal output to a level suitable for the modulator and the Matched coupling circuit.
2	Set the MG3670 series to the modulation system to be tested.
3	Set the MG3670 series modulation pattern to PN9 pseudorandom pattern.
4	Set the MS8604A so that the modulation system and pattern set in steps 2 and 3 can be received.
5	Using the MS8604A, measure the modulation accuracy and evaluate it. (For information on the MS8604A operation, refer to the MS8604A Operation Manual.)

SECTION 5
PERFORMANCE TESTS

This section describes the measuring instruments needed for performance tests, setup, and procedures using the MG0307A $\pi/4$ DQPSK Modulation Unit and the MG0303B Burst Function Unit in combination with the MG3670 series Digital Modulation Signal Generator. These performance tests are performed to check if the main performance parameters of the MG0307A and the MG0303B satisfy standard levels.

TABLE OF CONTENTS

5.1 Performance Tests Requirement 5-3

5.2 Instruments Required for Performance Tests 5-3

5.3 Performance Tests 5-4

5.3.1 I/Q signal modulation accuracy 5-4

5.3.2 RF output modulation accuracy 5-6

5.3.3 Modulation pattern 5-8

5.3.4 Burst signal On/Off ratio 5-9

5.3.5 Leakage power of adjacent channel characteristics 5-10

(Blank)

SECTION 5
PERFORMANCE TESTS

5.1 Performance Tests Requirement

Performance tests are performed as preventive maintenance to prevent performance deterioration. Performance tests are required at acceptance inspection, periodic inspection, and post-repair performance verification.

The following are the items that should be tested for verifying the performance of the MG0307A:

- I/Q signal modulation accuracy
- RF output modulation accuracy
- Modulation pattern

The following are the item that should be tested for verifying the performance of the MG0303B:

- Burst signal On/Off ratio

When used in combination with the MG3670B (main instrument), conduct the following performance test:

- Leakage power of adjacent channel characteristics

Execute performance tests periodically as preventive maintenance for important items. They should be executed at least once or twice a year to check performance. Contact the ANRITSU service department if the MG0307A or MG0303B fails to meet the specifications during performance tests.

5.2 Instruments Required for Performance Tests

The table below lists the measuring instruments required for the performance tests.

Recommended instrument (Anritsu model)	Required performance[†1]	Test items
Digital Mobile Radio Transmitter Tester (MS8604A)	400 kHz to 2.25 GHz[†2]	• I/Q signal modulation accuracy • RF output modulation accuracy
Data Transmission Analyzer (MD6420A)[†3]	42 to 1152 kbps	• Modulation pattern
Spectrum Analyzer (MS2602A)	300 kHz to 5 GHz	• Burst signal On/Off ratio

[†1] Only part of the performance that covers the test item measurement range is extracted.

[†2] The frequency upper limit conforms to specifications of the MG3670 series.

[†3] Error rate measuring instrument

5.3 Performance Tests

Before executing the performance tests explained on the following pages, unless otherwise specified, the instrument under test and all the other measuring instruments must be warmed-up for at least 30 minutes so the test is executed under stable conditions. To measure at the highest accuracy, the tests must be performed at room temperature, and ac power-supply voltage fluctuations must be minimized, and vibration and humidity must be kept at a reasonable level.

5.3.1 I/Q signal modulation accuracy

Verify the modulation accuracy of the I/Q signal output.

(1) Test specifications

- Modulation accuracy ..... 1.5 %rms (at 50 Ω、 500 mVrms output)

(2) Test instrument

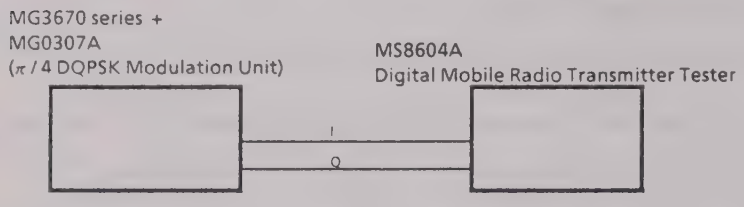
- Digital Mobile Radio Transmitter Tester MS8604A

  MS8604A options needed for measurement work:

  Option 03: IQ input ..... Used in the analysis of I/Q signals

  Option 12: PHP software ..... Used in the analysis of PHP signals

(3) Setup



(5) Test procedure

Step	Procedure
1	Set the MG3670 series I/Q output level to 50 Ω / 500 mVrms.
2	Set the MG3670 series to the modulation system to be tested.
3	Set the MG3670 series modulation pattern to PN9 pseudorandom pattern
4	Set the MS8604A so that the modulation system and pattern set in steps 2 and 3 can be received.
5	Using the MS8604A, measure the modulation accuracy and the I/Q signal.

Step	Procedure
	When an MG0303B burst function unit is installed, perform steps 6 to 9.
6	Set the MG3670 series burst function to On.
7	Set the modulation pattern to the communications channel.
8	Set the MS8604A so that the pattern set in step 7 can be received.
9	Using the MS8604A, measure the modulation accuracy and the I/Q signal.. (For information on the MS8604A operation, refer to the MS8604A Operation Manual.)

5.3.2 RF output modulation accuracy

Verify the modulation accuracy of the RF modulation signal output.

(1) Test specifications

- Frequency range ..... 1 MHz to 2.25 GHz† (PACS, PHS)
  5 MHz to 2.25 GHz† (WCPE)
- Modulation accuracy ..... 1.8% rms (at ≦ +5 dBm output level)

†: The frequency upper limit conforms to specifications of the MG3670 series.

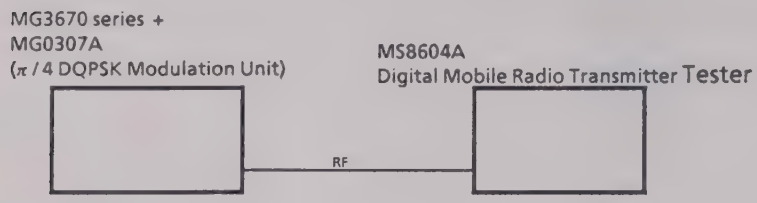
(2) Test instrument

- Digital Mobile Radio Transmitter Tester MS8604A

MS8604A options needed for measurement work:

Option 12: PHP software ..... Used in the analysis of PHS signals

(3) Setup



(4) Test procedure

Step	Procedure
1	Set the MG3670 series to the frequency to be tested.
2	Set the MG3670 series output level to +5 dBm.
3	Set the MG3670 series to the modulation system to be tested.
4	Set the MG3670 series modulation pattern to PN9 pseudorandom pattern
5	Set the MS8604A so that the modulation system and pattern set in steps 3 and 4 can be received.
6	Using the MS8604A, measure the modulation accuracy of the RF modulation signal.
	When an MG0303B burst function unit is installed, perform steps 7 to 10
7	Set the MG3670 series burst function to On.
8	Set the modulation pattern to the communications channel.
9	Set the MS8604A so that the pattern set in step 8 can be received.
10	Using the MS8604A, Measure the modulation accuracy of the RF modulation signal (For information on the MS8604A operation, refer to the MS8604A Operation Manual.)

5.3.3 Modulation pattern

Verify the modulation pattern.

(1) Test specifications

- PN9 and PN15 pseudorandom pattern ..... Burst function Off
- PN9 and PN15 pseudorandom pattern on slot ..... Burst function On

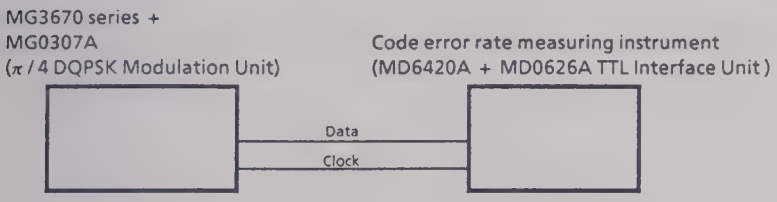
(2) Test instrument

- Data Transmission Analyzer MD6420A

MD6420A unit needed for measurement work:

MD0626A ..... TTL Interface Unit

(3) Setup



(4) Test procedure

Step	Procedure
1	Set the MG3670 series to the modulation system to be tested.
2	Set the MG3670 series modulation pattern to PN9/PN15 pseudorandom pattern.
3	Connect the MG3670 series data output and data clock to the code error rate measuring instrument. (Connect the data and the clock to the RD (Data) and RT (clock) connectors of the TTL Interface Unit (MD0626A) inserted on the MD6420A rear panel, respectively.)
4	Set the MD6420A receive timing to RT (INV) mode.
5	Set the MD6420A pattern to 2^9-1 (PN9) and $2^{15}-1$ (PN15).
6	Press the MD6420A MEAS key to measure the code error rate.
	When the MG0303B burst function unit is installed, perform steps 7 to 12.
7	Set the MG3670 series burst function to On.
8	Set the modulation pattern to the communications channel.
9	Set TCH (Traffic Channel) to PN9/PN15 pseudorandom pattern.
10	Set the Pattern Sync output signal to PN Clock.
11	Set the MD6420A pattern to 2^9-1 (PN9) and $2^{15}-1$ (PN15).
12	Press the MD6420A MEAS key to measure the code error rate.

Note: • *Set the polarity of the MG3670 series data output to positive.*
• *(For information on the MD6420A operation, refer to the MD6420A Operation Manual.)*

5.3.4 Burst signal On/Off ratio

Verify the On/Off ratio of the burst signal output.

(1) Test specifications

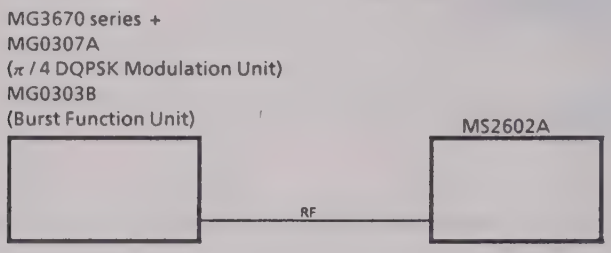
- Frequency range ..... 1 MHz to 2.25 GHz† (PACS, PHS)
  5 MHz to 2.25 GHz† (WCPE)
- On/Off ratio ..... ≧75 dB: At 5 dBm output (PACS, PHS)
  ≧70 dB: At 5 dBm output (WCPE)

†: The frequency upper limit conforms to specifications of the MG3670 series.

(2) Test instrument

- Spectrum analyzer MS2602A

(3) Setup



(4) Test procedure

Step	Procedure
1	Set the MG3670 series to the frequency to be tested.
2	Set the MG3670 series output level to +5 dBm.
3	Set the MG3670 series to the modulation system to be tested.
4	Set the MG3670 series burst function to On.
5	Set the MS2602A to the frequency to be tested.
6	Set the MS2602A sweep frequency width to 0 Hz, and observe the output level on and off condition in the time domain.
7	Set the MS2602A parameters to suitable levels, and measure the On and Off ratio. *(For information on the MS2602A operation, refer to the MS2602A Operation Manual.)*

Step Procedure

In addition, examples of the MS2602A setting parameters are shown in the table below. Use video average function when you perform a measurement.

COMMUNICATIONS SYSTEM	RBW	VBW	SWEEP TIME	REFERENCE LEVEL	ATT
PACS	100 kHz	3 MHz	1 ms	5 dBm	15 dB
PHS	100 kHz	3 MHz	1 ms	5 dBm	15 dB
WCPE	100 kHz	3 MHz	1 ms	0 dBm	10 dB

5.3.5 Leakage power of adjacent channel characteristics

Check the leakage power of adjacent channel characteristics as instructed below.

(1) Test specifications

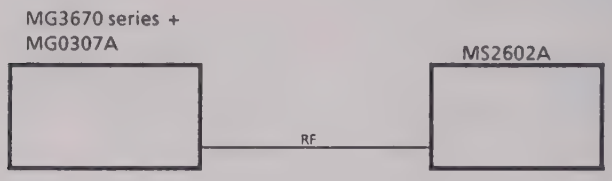
- Frequency range ..... 1 to 2.25 GHz† (PHS)
- Leakage power of adjacent channel ratio ..... ≦ −70 dB: 600 kHz offset, ±96 kHz bandwidth
  ≦ −70 dB: 900 kHz offset, ±96 kHz bandwidth

†: The frequency upper limit conforms to specifications of the MG3670 series.

(2) Test instrument

- Spectrum analyzer MS2602A
  (with leakage power of adjacent channel measurement function)

(3) Setup



(4) Test procedure

Step	Procedure
1	Set the MG3670 series to the frequency to be tested.
2	Set the output level, for example, to −10 dBm.
3	Set the modulation to On and the communications system to PHS.
4	Set the modulation pattern to PN9. For a model with burst function, conduct the test with the burst function set to On.
5	Set the MS2602A to the frequency of Step 1.
6	Set the MS2602A sweep frequency width to about 2 MHz.
7	Set the MS2602A sweep time to 5 s or more.
8	Set other parameters of the MS2602A to optimum levels.
9	Measure the leakage power of adjacent channel ratio using the leakage power of adjacent channel ratio measurement function. (For information on the MS2602A operation, refer to the MS2602A Operation Manual.)

MG0307A

π/4 DQPSK Modulation Unit

Operation Manual
(GPIB Remote Control)

(Blank)

CERTIFICATION

ANRITSU CORPORATION certifies that this instrument has been thoroughly tested and inspected, and found to meet published specifications prior to shipping.
Anritsu further certifies that its calibration measurements are based on the Japanese Electrotechnical Laboratory and Radio Research Laboratory standards.

WARRANTY

All parts of this product are warranted by Anritsu Corporation of Japan against defects in material or workmanship for a period of one year from the date of delivery.
In the event of a defect occurring during the warranty period, Anritsu Corporation will repair or replace this product within a reasonable period of time after notification, free-of-charge, provided that: it is returned to Anritsu; has not been misused; has not been damaged by an act of God; and that the user has followed the instructions in the operation manual.

Any unauthorized modification, repair, or attempt to repair, will render this warranty void.

This warranty is effective only for the original purchaser of this product and is not transferable if it is resold.

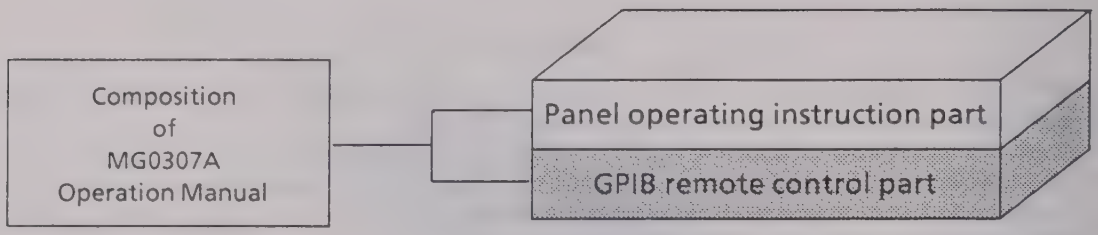
ALL OTHER EXPRESSED WARRANTIES ARE DISCLAIMED AND ALL IMPLIED WARRANTIES FOR THIS PRODUCT, INCLUDING THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE LIMITED IN DURATION TO A PERIOD OF ONE YEAR FROM THE DATE OF DELIVERY. IN NO EVENT SHALL ANRITSU CORPORATION BE LIABLE TO THE CUSTOMER FOR ANY DAMAGES, INCLUDING LOST PROFITS, OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES, ARISING OUT OF THE USE OR INABILITY TO USE THIS PRODUCT.

All requests for repair or replacement under this warranty must be made as soon as possible after the defect has been noticed and must be directed to Anritsu Corporation or its representative in your area.

ABOUT THIS MANUAL

(1) Composition of MG0307A Operation Manuals

The MG0307A π/4DQPSK Modulation Unit operation manual is composed of the following two parts. Use them properly according to the usage purpose.



Panel operating instruction part: Provides information on the MG0307A outline, preparation before use, manual operation, measuremant, performance test, storage, transportation, communication system, frame composition diagram, and the MG0303B Burst Function Unit when operated with the MG0307A.

GPIB remote control part: Provides information on the MG0307A remote control which conforms with IEEE488.2 standards. To assist creating GPIB programs, this manual gives examples of N_{88} BASIC language programs that run on the NEC PC9800 series of personal computers.

The operation manual of the MG3670 series Digital Modulation Signal Generator in which the MG0307A is incorporated is prepared and sold separately. It is recommended that the MG3670 series operation manual should also be read with this manual.

(2) GPIB Basic Guide (sold separately)

The GPIB Basic Guide is sold separately in addition to the above GPIB operation manual. It is composed of two parts: GPIB Basic Knowledge, and GPIB Control statements in the ANRITSU PACKET V BASIC.

TABLE OF CONTENTS

1 GENERAL 1-1

2 MG0307A DEVICE MESSAGE LIST 2-1

2.1 How to Read the MG0307A Device Message List 2-1
2.2 MG0307A Device Message List 2-2

3 DETAILED DESCRIPTION OF COMMANDS 3-1

4 SAMPLE PROGRAMS 4-1

4.1 Generating π/4DQPSK Modulation Signal 4-1
4.2 Setting the Internal Modulation Data 4-2

(Blank)

1. GENERAL

The MG0307A π/4DQPSK Modulation Unit is one of the units used with the MG3670 series Digital Modulation Signal Generator.

This GPIB remote control part provides the MG0307A device message list, its detailed descriptions , and some sample programs with those commands specific to the MG0307A.

For other description of GPIB, refer to the GPIB Remote Control part in the MG3670 series Digital Modulation Signal Generator Operation Manual.

(Blank)

2. MG0307A DEVICE MESSAGE LIST

The tables on the following pages list the command messages, query messages, and response messages specific to the MG0307A π/4DQPSK Modulation Unit.

2.1 How to Read the MG0307A Device Message List

(1) Command Messages (Command Msg)/Query Message (Query Msg)

(a) Upper-case:	Reserved word
(b) Number:	Reserved word (Number code)
(c) Lower-case argument	
n (Integral number):	Numeric data (NR1 format)
h (hexadecimal number):	Numeric data (hexadecimal data)
s:	Character string enclosed by double quotation marks (" ") or single quotation marks (' ')

(2) Response message (Response Msg)

(a) Upper-case:	Reserved word
(b) Number:	Reserved word (Number code)
(c) Lower-case argument	
n (Integral number):	Numeric data (NR1 format)
h (hexadecimal number):	Numeric data (hexadecimal data)

Note: • *If the header is set to Off, then the response message header and the numeric data suffix code are not transferred. (Initial setting: Header Off)*

• ␣ *means a space of one character.*

• Ø *indicates a zero.*

2.2 MG0307A Device Message List

(1) Modulation

Measurement paramete		Command Msg	Query Msg	Response Msg
Brief Function	Control Item			
Sets I, Q signal source	Modulation Mode Source			
	I, Q Int	MODE␣INT	MODE?	MODE␣INT
	I, Q Ext	MODE␣EXT	MODE?	MODE␣EXT
Sets nyquist filter type	Nyquist Filter Type			
	Root Nyquist	NYQ␣R	NYQ?	NYQ␣R
	Nyquist	NYQ␣N	NYQ?	NYQ␣N
Differential phase encoding	Differential Phase Encoding			
	Normal	DPE␣NORM	DPE?	DPE␣NORM
	Invers	DPE␣INVS	DPE?	DPE␣INVS
Sets internal modulation data (BURST Off)	PACS / PHS			
	Pattern			
	0000	PAT␣0000	PAT?	PAT␣0000
	0001	PAT␣0001	PAT?	PAT␣0001
	0010	PAT␣0010	PAT?	PAT␣0010
	0011	PAT␣0011	PAT?	PAT␣0011
	0100	PAT␣0100	PAT?	PAT␣0100
	0101	PAT␣0101	PAT?	PAT␣0101
	0110	PAT␣0110	PAT?	PAT␣0110
	0111	PAT␣0111	PAT?	PAT␣0111
	1000	PAT␣1000	PAT?	PAT␣1000
	1001	PAT␣1001	PAT?	PAT␣1001
	1010	PAT␣1010	PAT?	PAT␣1010
	1011	PAT␣1011	PAT?	PAT␣1011
	1100	PAT␣1100	PAT?	PAT␣1100
	1101	PAT␣1101	PAT?	PAT␣1101
	1110	PAT␣1110	PAT?	PAT␣1110
	1111	PAT␣1111	PAT?	PAT␣1111
	PN15	PAT␣PN15	PAT?	PAT␣PN15
	PN9	PAT␣PN9	PAT?	PAT␣PN9
	WCPE			
	Pattern			
	0000 ~ FFFF	PAT␣h	PAT?	PAT␣h
	PN15	PAT␣PN15	PAT?	PAT␣PN15
	PN9	PAT␣PN9	PAT?	PAT␣PN9
Turns Burst function on or off	Burst			
	On	BST␣ON	BST?	BST␣ON
	Off	BST␣OFF	BST?	BST␣OFF

(Continued)

Measurement paramete		Command Msg	Query Msg	Response Msg
Brief Function	Control Item			
Sets burst trigger source	Burst Trigger Int Ext	 BTG␣INT BTG␣EXT	 BTG? BTG?	 BTG␣INT BTG␣EXT
Changes symbol adjust state	Symbol Adjust	SAD	———	———
Sets timing of the burst trigger	Burst Trigger Select Uplink Downlink	 TGS␣UP TGS␣DN	 TGS? TGS?	 TGS␣UP TGS␣DN

(2) Internal modulation data

Measurement paramete		Command Msg	Query Msg	Response Msg
Brief Function	Control Item			
Selects communication systems	System PACS PHS WCPE	 SYS␣PACS SYS␣PHS SYS␣WCPE	 SYS? SYS? SYS?	 SYS␣PACS SYS␣PHS SYS␣WCPE
Sets internal modulation data (BURST ON)	Pattern			
	PACS UP DEVICE UP TCH UP TCH ALL DN TCH DN TCH ALL	 PAT␣UPDV PAT␣UPT PAT␣UPTA PAT␣DNT PAT␣DNTA	 PAT? PAT? PAT? PAT? PAT?	 PAT␣UPDV PAT␣UPT PAT␣UPTA PAT␣DNT PAT␣DNTA
	PHS UP DEVICE DOWN DEVICE UP TCH UP TCH ALL DOWN TCH DOWN TCH ALL UP VOX DOWN VOX UP SYNC DOWN SYNC	 PAT␣UPDV PAT␣DNDV PAT␣UPT PAT␣UPTA PAT␣DNT PAT␣DNTA PAT␣UPVX PAT␣DNVX PAT␣UPSYNC PAT␣DNSYNC	 PAT? PAT? PAT? PAT? PAT? PAT? PAT? PAT? PAT? PAT?	 PAT␣UPDV PAT␣DNDV PAT␣UPT PAT␣UPTA PAT␣DNT PAT␣DNTA PAT␣UPVX PAT␣DNVX PAT␣UPSYNC PAT␣DNSYNC

(Continued)

Measurement paramete		Command Msg	Query Msg	Response Msg
Brief Function	Control Item			
Sets internal modulation data (BURST On) (Continued)	Pattern			
	WCPE			
	Full Solt			
	UP DEV P00	PAT␣UPDP00	PAT?	PAT␣UPDP00
	UP DEV P00 S	PAT␣UPDP00S	PAT?	PAT␣UPDP00S
	UP DEV P32	PAT␣UPDP32	PAT?	PAT␣UPDP32
	UP DEV P32 S	PAT␣UPDP32S	PAT?	PAT␣UPDP32S
	UP P00	PAT␣UPP00	PAT?	PAT␣UPP00
	UP P00 ALL	PAT␣UPP00A	PAT?	PAT␣UPP00A
	UP P32	PAT␣UPP32	PAT?	PAT␣UPP32
	UP P32 ALL	PAT␣UPP32A	PAT?	PAT␣UPP32A
	DN DEV P00	PAT␣DNDP00	PAT?	PAT␣DNDP00
	DN DEV P00 S	PAT␣DNDP00S	PAT?	PAT␣DNDP00S
	DN DEV P32	PAT␣DNDP32	PAT?	PAT␣DNDP32
	DN DEV P32 S	PAT␣DNDP32S	PAT?	PAT␣DNDP32S
	DN P00	PAT␣DNP00	PAT?	PAT␣DNP00
	DN P00 ALL	PAT␣DNP00A	PAT?	PAT␣DNP00A
	DN P32	PAT␣DNP32	PAT?	PAT␣DNP32
	DN P32 ALL	PAT␣DNP32A	PAT?	PAT␣DNP32A
	Duble Slot			
	UP DEV P80	PAT␣UPDP80	PAT?	PAT␣UPDP80
	UP DEV P80 S	PAT␣UPDP80S	PAT?	PAT␣UPDP80S
	UP P80	PAT␣UPP80	PAT?	PAT␣UPP80
	UP P80 ALL	PAT␣UPP80A	PAT?	PAT␣UPP80A
	DN DEV P80	PAT␣DNDP80	PAT?	PAT␣DNDP80
	DN DEV P80 S	PAT␣DNDP80S	PAT?	PAT␣DNDP80S
	DN P80	PAT␣DNP80	PAT?	PAT␣DNP80
	DN P80 ALL	PAT␣DNP80A	PAT?	PAT␣DNP80A
	Half Slot			
	UP DEV P08	PAT␣UPDP08	PAT?	PAT␣UPDP08
	UP DEV P08 S	PAT␣UPDP08S	PAT?	PAT␣UPDP08S
	UP P08	PAT␣UPP08	PAT?	PAT␣UPP08
	UP P08 ALL	PAT␣UPP08A	PAT?	PAT␣UPP08A
	DN DEV P08	PAT␣DNDP08	PAT?	PAT␣DNDP08
	DN DEV P08 S	PAT␣DNDP80S	PAT?	PAT␣DNDP80S
	DN P08	PAT␣DNP08	PAT?	PAT␣DNP08
	DN P08 ALL	PAT␣DNP08A	PAT?	PAT␣DNP08A
	Memory	PAT␣MEMn	PAT?	PAT␣MEMn

(3) Setting the slot

Measurement paramete		Command Msg	Query Msg	Response Msg
Brief Function	Control Item			
Selects slot number	PACS / PHS Select Slot Number WCPE Full Slot Select Slot Number (n=0, 1, 2, ···, 23) Double Slot Select Slot Number (n=0, 2, 4, 6, ···, 22) Half Slot Select Slot Number (n=0, 1, 2, ···, 23) (m=0, 1)	SLOTNO␣n SLOTNO␣n SLOTNO␣n SLOTNO␣n,m	SLOTNO? SLOTNO? SLOTNO? SLOTNO?	SLOTNO␣n SLOTNO␣n SLOTNO␣n SLOTNO␣n,m
Sets the slot	Modify Slot			
	PACS UP DEVICE: On Off UP TCH: UP TCH Off UP TCH ALL: UP TCH Off DOWN TCH: DOWN TCH Off DOWN TCH ALL: DOWN TCH Off	 SLOT␣UPDV SLOT␣OFF SLOT␣UPT SLOT␣OFF SLOT␣UPT SLOT␣OFF SLOT␣DNT SLOT␣OFF SLOT␣DNT SLOT␣OFF		
	PHS UP DEVICE: On Off DOWN DEVICE: On Off UP TCH: On Off	 SLOT␣ON SLOT␣OFF SLOT␣ON SLOT␣OFF SLOT␣ON SLOT␣OFF	 SLOT? SLOT? SLOT? SLOT? SLOT? SLOT?	 SLOT␣ON SLOT␣OFF SLOT␣ON SLOT␣OFF SLOT␣ON SLOT␣OFF

(Continued)

Measurement paramete		Command Msg	Query Msg	Response Msg
Brief Function	Control Item			
Sets the slot (Continued)	UP TCH ALL:			
	On	SLOT␣ON	SLOT?	SLOT␣ON
	Off	SLOT␣OFF	SLOT?	SLOT␣OFF
	DOWN TCH:			
	DOWN TCH	SLOT␣DNT	SLOT?	SLOT␣DNT
	VOX	SLOT␣VOX	SLOT?	SLOT␣VOX
	Off	SLOT␣OFF	SLOT?	SLOT␣OFF
	DOWN TCH ALL:			
	DOWN TCH	SLOT␣DNT	SLOT?	SLOT␣DNT
	VOX	SLOT␣VOX	SLOT?	SLOT␣VOX
	Off	SLOT␣OFF	SLOT?	SLOT␣OFF
	UP VOX:			
	On	SLOT␣ON	SLOT?	SLOT␣ON
	Off	SLOT␣OFF	SLOT?	SLOT␣OFF
	DOWN VOX:			
	DOWN TCH	SLOT␣DNT	SLOT?	SLOT␣DNT
	VOX	SLOT␣VOX	SLOT?	SLOT␣VOX
	Off	SLOT␣OFF	SLOT?	SLOT␣OFF
	UP SYNC:			
	UP TCH	SLOT␣UPT	SLOT?	SLOT␣UPT
	UP SYNC	SLOT␣UPSYNC	SLOT?	SLOT␣UPSYNC
	Off	SLOT␣OFF	SLOT?	SLOT␣OFF
	DOWN SYNC:			
	DOWN TCH	SLOT␣DNT	SLOT?	SLOT␣DNT
	DOWN SYNC	SLOT␣DNSYNC	SLOT?	SLOT␣DNSYNC
	VOX	SLOT␣VOX	SLOT?	SLOT␣VOX
	Off	SLOT␣OFF	SLOT?	SLOT␣OFF
	WCPE			
	Full Slot			
	DEV P00	SLOT␣DPØØ	SLOT?	SLOT␣DPØØ
	DEV P32	SLOT␣DP32	SLOT?	SLOT␣DP32
	DEV P00 S	SLOT␣DPØØS	SLOT?	SLOT␣DPØØS
	DEV P32 S	SLOT␣DP32S	SLOT?	SLOT␣DP32S
	P00	SLOT␣PØØ	SLOT?	SLOT␣PØØ
	P32	SLOT␣P32	SLOT?	SLOT␣P32
	Off	SLOT␣OFF	SLOT?	SLOT␣OFF
	Double Slot			
	DEV P80	SLOT␣DP8Ø	SLOT?	SLOT␣DP8Ø
	DEV P80 S	SLOT␣DP8ØS	SLOT?	SLOT␣DP8ØS
	P80	SLOT␣P8Ø	SLOT?	SLOT␣P8Ø
	Off	SLOT␣OFF	SLOT?	SLOT␣OFF
	Half Slot			
	DEV P08	SLOT␣DPØ8	SLOT?	SLOT␣DPØ8
	DEV P08 S	SLOT␣DPØ8S	SLOT?	SLOT␣DPØ8S
	P08	SLOT␣PØ8	SLOT?	SLOT␣PØ8
	Off	SLOT␣OFF	SLOT?	SLOT␣OFF

(4) Setting data of the pattern

Measurement paramete		Command Msg	Query Msg	Response Msg
Brief Function	Control Item			
Sets data of the pattern	Pattern Edit			
	PACS			
	DEVICE			
	PN			
	PN9	PN␣PN9	PN?	PN␣PN9
	PN15	PN␣PN15	PN?	PN␣PN15
	UP TCH			
	DE (0h ~ 3h)	DE␣h	DE?	DE␣h
	SC (000h ~ 3FFh)	SC␣h	SC?	SC␣h
	FC			
	PN9	FCH␣PN9	FCH?	FCH␣PN9
	PN15	FCH␣PN15	FCH?	FCH␣PN15
	ALL '0'	FCH␣ALLØ	FCH?	FCH␣ALLØ
	ALL '1'	FCH␣ALL1	FCH?	FCH␣ALL1
	R (0h ~ 1h)	R␣h	R?	R␣h
	DOWN TCH			
	SYC (0000h ~ 3FFFh)	SYC␣h	SYC?	SYC␣h
	SC (000h ~ 3FFh)	SC␣h	SC?	SC␣h
	FC			
	PN9	FCH␣PN9	FCH?	FCH␣PN9
	PN15	FCH␣PN15	FCH?	FCH␣PN15
	ALL '0'	FCH␣ALLØ	FCH?	FCH␣ALLØ
	ALL '1'	FCH␣ALL1	FCH?	FCH␣ALL1
	PCC (0h ~ 1h)	PCC␣h	PCC?	PCC␣h
	Pattern Edit			
	PHS			
	DEVICE			
	PN			
	PN9	PN␣PN9	PN?	PN␣PN9
	PN15	PN␣PN15	PN?	PN␣PN15
	TCH			
	UW (0000h ~ FFFFh)	UW␣h	UW?	UW␣h
	SA (0000h ~ FFFFh)	SA␣h	SA?	SA␣h
	TCH			
	PN9	TCH␣PN9	TCH?	TCH␣PN9
	PN15	TCH␣PN15	TCH?	TCH␣PN15
	CS-ID Scramble			
	On	SCBL␣ON	SCBL?	SCBL␣ON
	Off	SCBL␣OFF	SCBL?	SCBL␣OFF

(Continued)

Measurement paramete		Command Msg	Query Msg	Response Msg
Brief Function	Control Item			
Sets data of the pattern (Continued)	CS-ID Code (000h ~ 3FFh)	SCBLC␣h	SCBLC?	SCBLC␣h
	Secret Scramble			
	On	SCRT␣ON	SCRT?	SCRT␣ON
	Off	SCRT␣OFF	SCRT?	SCRT␣OFF
	Secret Code (0000h ~ FFFFh)	SCRTC␣h	SCRTC?	SCRTC␣h
	VOX			
	UW (0000h ~ FFFFh)	UW␣h	UW?	UW␣h
	SA (0000h ~ FFFFh)	SA␣h	SA?	SA␣h
	VOX			
	PN9	VOX␣PN9	VOX?	VOX␣PN9
	PN15	VOX␣PN15	VOX?	VOX␣PN15
	CS-ID Scramble			
	On	SCBL␣ON	SCBL?	SCBL␣ON
	Off	SCBL␣OFF	SCBL?	SCBL␣OFF
	CS-ID Code (000h ~ 3FFh)	SCBLC␣h	SCBLC?	SCBLC␣h
	Secret Scramble			
	On	SCRT␣ON	SCRT?	SCRT␣ON
	Off	SCRT␣OFF	SCRT?	SCRT␣OFF
	Secret Code (0000h ~ FFFFh)	SCRTC␣h	SCRTC?	SCRTC␣h
	SYNC			
	UW (0000h ~ FFFFh)	UW␣h	UW?	UW␣h
	CI (0h ~ Fh)	CI␣h	CI?	CI␣h
	CS-ID (00000000000h ~ 3FFFFFFFFFFh)	CSID␣h	CSID?	CSID␣h
	PS-ID (0000000h ~ FFFFFFFh)	PSID␣h	PSID?	PSID␣h
	Idle (000000000h ~ 3FFFFFFFFh)	IDLE␣h	IDLE?	IDLE␣h
	Scramble			
	On	SCBL␣ON	SCBL?	SCBL␣ON
	Off	SCBL␣OFF	SCBL?	SCBL␣OFF
	Scramble Code (000h ~ 3FFh)	SCBLC␣h	SCBLC?	SCBLC␣h

(Continued)

Measurement paramete		Command Msg	Query Msg	Response Msg
Brief Function	Control Item			
Sets data of the pattern	WCPE Edit Data DEV P00 / DEV P32 / DEV P80 / DEV P08 DATA			
	PN9	DATA␣PN9	DATA?	DATA␣PN9
	PN15	DATA␣PN15	DATA?	DATA␣PN15
	ALL '0'	DATA␣ALLØ	DATA?	DATA␣ALLØ
	ALL '1'	DATA␣ALL1	DATA?	DATA␣ALL1
	DEV P00 S S (00000000h ~ FFFFFFFFh) DATA	S␣h	S?	S␣h
	PN9	DATA␣PN9	DATA?	DATA␣PN9
	PN15	DATA␣PN15	DATA?	DATA␣PN15
	ALL '0'	DATA␣ALLØ	DATA?	DATA␣ALLØ
	ALL '1'	DATA␣ALL1	DATA?	DATA␣ALL1
	DEV P32 / DEV P80 S / DEV P08 S S (00000000h ~ FFFFFFFFh) DATA	S␣h	S?	S␣h
	PN9	DATA␣PN9	DATA?	DATA␣PN9
	PN15	DATA␣PN15	DATA?	DATA␣PN15
	ALL '0'	DATA␣ALLØ	DATA?	DATA␣ALLØ
	ALL '1'	DATA␣ALL1	DATA?	DATA␣ALL1
	Z			
	On	Z␣ON	Z?	Z␣ON
	Off	Z␣OFF	Z?	Z␣OFF
	P00 S (00000000h ~ FFFFFFFFh)	S␣h	S?	S␣h
	H (00h ~ FFh)	H␣h	H?	H␣h
	T is divided into TQ and TC, and set to TQ or TC.			
	TQ (00h ~ FFh)	TQ␣h	TQ?	TQ␣h
	TC			
	PN9	TC␣PN9	TC?	TC␣PN9
	PN15	TC␣PN15	TC?	TC␣PN15
	h (00000000h ~ FFFFFFFFh)	TC␣h	TC?	TC␣h

(Continued)

Measurement paramete		Command Msg	Query Msg	Response Msg
Brief Function	Control Item			
Sets data of the pattern (Continued)	P32 / P80 / P08			
	S (00000000h ~ FFFFFFFFh)	S␣h	S?	S␣h
	H (00h ~ FFh)	H␣h	H?	H␣h
	T is divided into TQ and TC, and set to TQ or TC.			
	TQ (00h ~ FFh)	TQ␣h	TQ?	TQ␣h
	TC			
	h (00000000h ~ FFFFFFFFh)	TC␣h	TC?	TC␣h
	DATA			
	PN9	DATA␣PN9	DATA?	DATA␣PN9
	PN15	DATA␣PN15	DATA?	DATA␣PN15
	TEST PATT	DATA␣TEST	DATA?	DATA␣TEST
	REP PATT (00h ~ FFh)	DATA␣h	DATA?	DATA␣h
	Z			
	On	Z␣ON	Z?	Z␣ON
	Off	Z␣OFF	Z?	Z␣OFF

(5) Save / Recall

Measurement paramete		Command Msg	Query Msg	Response Msg
Brief Function	Control Item			
Saves burst internal modulation data	Burst Pattern Memory Save	BSAV␣n[,s]†	———	———

† It is possible to omit 's'(Title).

3. DETAILED DESCRIPTION OF COMMANDS

This section describes in detail the device messages for MG0307A π/4DQPSK Modulation Unit. The device messages are listed in alphabetical.

TABLE OF CONTENTS

BSAV 3-3
BST 3-3
BTG 3-4
CI 3-5
CSID 3-5
DATA 3-6
DE 3-6
DPE 3-7
FCH 3-8
H 3-9
IDLE 3-10
MODE 3-11
NYQ 3-12
PAT 3-13
PAT 3-14
PAT 3-15
PCC 3-15
PN 3-16
PSID 3-16
R 3-17
S 3-18
SA 3-18
SAD 3-19
SC 3-19
SCBL 3-20
SCBLC 3-20
SCRT 3-21
SCRTC 3-21
SLOT 3-22
SLOTNO 3-24
SYC 3-24
SYS 3-25
TC 3-26
TCH 3-26
TGS 3-27
TQ 3-27
UW 3-28

TABLE OF CONTENTS (Continued)

VOX 3-29
Z 3-30

BSAV Burst Pattern Memory Save

■ Function

Saves the burst internal modulation data to burst pattern memory.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
BSAV	BSAV␣a[,b]	———	———

■ Value of a Ø to 99

■ Value of b Character string whithin 8 characters enclosed by double quotation marks or single quotation marks.
Saves the title which is sets currently if b is omitted.
Saves the first eight characters of b if b is over eight characters.

■ Suffix code None

■ Example BSAV␣5, "MG367ØB"

BST Burst On/Off

■ Function

Turns the Burst function on or off.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
BST	BST␣a	BST?	BST␣a

■ Value of a ON: On
OFF: Off

■ Suffix code None

■ Initial setting OFF

■ Example BST␣ON

BTG Burst Trigger Source

■ Function Sets the burst trigger source to either internal (Int) or external (Ext). (When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
BTG	BTG␣a	BTG?	BTG␣a

■ Value of a
INT: Internal burst trigger
EXT: External burst trigger

■ Suffix code None

■ Initial setting INT

■ Example BTG␣EXT

CI Channel Identifier

■ Function — Sets the CI data of SYNC slot in the PHS system.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
CI	CI␣a	CI?	CI␣a

■ Value of a — #HØ to #HF (Hexadecimal number)
■ Suffix code — None
■ Initial setting — #H9
■ Example — CI␣#HF

CSID CS Identification Code

■ Function — Sets the CS-ID data of SYNC slot in the PHS system.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
CSID	CSID␣a	CSID?	CSID␣a

■ Value of a — #HØØØØØØØØØØØ to #H3FFFFFFFFFF (Hexadecimal number)
■ Suffix code — None
■ Initial setting — #H20200020001
■ Example — CSID␣#H20200020003

D

DATA Data

■ Function

Sets the DATA data of the solot in the WCPE system.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
DATA	DATA␣a	DATA?	DATA␣a

■ Value of a

For device evaluation slot (At DEV P00, DEV P32, DEV P80, DEV P08)

```
PN9:    PN9
PN15:   PN15
ALL1:   ALL'1'
ALLØ:   ALL'Ø'
```

For communication channel slot (At P32, P80, P08)

```
PN9:    PN9
PN15:   PN15
TEST:   TEST PATT
h:      REP PATT
```

■ Suffix code None

■ Initial setting PN9

■ Example DATA␣PN15

DE Differential Encode

■ Function

Sets the DE data of the uplink communications channel in the PACS system.
(When the burst function unit is supported, this function is available.)

Header	Program command	Query	Response
DE	DE␣a	DE?	DE␣a

■ Value of a #HØ to #H3 (Hexa decimal number)

■ Suffix code None

■ Initial setting #HØ

■ Example DE␣#H3

DPE Differential Phase Encoding

■ Function

Sets the differential phase encoding specifications for $\pi / 4$ DQPSK modulation when a $\pi / 4$ DQPSKmodulation system is selected.

Header	Program command	Query	Response
DPE	DPE␣a	DPE?	DPE␣a

■ Value of a

NORM: Normal
INVS: Invers (inverted differential phase encoding)

■ Suffix code

None

■ Initial setting

NORM

■ Example

DPE␣INVS

FCH Fast Channel

■ Function Sets the FC data of the uplink/downlink communications channels in the PACS system.
(When the burst function unit is supported, this function is available.)

Header	Program command	Query	Response
FCH	FCH␣a	FCH?	FCH␣a

■ Value of a PN9, PN15, ALLØ, ALL1

■ Suffix code None

■ Initial setting PN9

■ Example FCH␣PN15

H Header

■ Function Sets the H data of the slot in the WCPE system.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
H	H␣a	H?	H␣a

■ Value of a #HØØ to #HFF

■ Suffix code None

■ Initial setting #HCE

■ Example H␣#HCB

IDLE Idle Bit

■ Function Sets the Idle data of SYNC slot in the PHS system.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
IDLE	IDLE␣a	IDLE?	IDLE␣a

■ Value of a #H00000000 to #H3FFFFFFF (Hexadecimal number)

■ Suffix code None

■ Initial setting #H00000000

■ Example IDLE␣#H3AAAAAAA

MODE Modulation Mode Source

■ Function Sets the I,Q signals source to either internal (Int) or external (Ext).

Header	Program command	Query	Response
MODE	MODE␣a	MODE?	MODE␣a

■ Value of a
INT: Internal I,Q signals
EXT: External I,Q signals

■ Suffix code None

■ Initial setting INT

■ Example MODE␣EXT

NYQ Nyquist Filter Type

■ Function Sets the nyquist filter type to either Root Nyquist or Nyquist .

Header	Program command	Query	Response
NYQ	NYQ␣a	NYQ?	NYQ␣a

■ Value of a
R: Root Nyquist
N: Nyquist

■ Suffix code None

■ Initial setting R

■ Example NYQ␣N

PAT Pattern

■ Function

Sets the internal modulation data pattern when the burst function turns on. (When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
PAT	PAT␣a	PAT?	PAT␣a

■ Value of a

When system is PACS

UPDV:	UP DEVICE
UPT:	UP TCH
UPTA:	UP TCH ALL
DNT:	DOWN TCH
DNTA:	DOWN TCH ALL

When system is PHS

UPDV:	UP DEVICE
DNDV:	DOWN DEVICE
UPT:	UP TCH
UPTA:	UP TCH ALL
DNT:	DOWN TCH
DNTA:	DOWN TCH ALL
UPVX:	UP VOX
DNVX:	DOWN VOX
UPSYNC:	UP SYNC
DNSYNC:	DOWN SYNC

When system is WCPE
AT Full Slot

UPDPØØ:	UP DEV PØØ
UPDPØØS:	UP DEV PØØ S
UPDP32:	UP DEV P32
UPDP32S:	UP DEV P32 S
UPPØØ:	UP PØØ
UPPØØA:	UP PØØ ALL
UPP32:	UP P32
UPP32A:	UP P32 ALL
DNDPØØ:	DN DEV PØØ
DNDPØØS:	DN DEV PØØ S
DNDP32:	DN DEV P32
DNDP32S:	DN DEV P32 S
DNPØØ:	DN PØØ
DNPØØA:	DN PØØ ALL
DNP32:	DN P32
DNP32A:	DN P32 ALL

At Double Slot

```
UPDP8Ø:    UP DEV P8Ø
UPDP8ØS:   UP DEV P8Ø S
UPP8Ø:     UP P8Ø
UPP8ØA:    UP P8Ø ALL
DNDP8Ø:    DN DEV P8Ø
DNDP8ØS:   DN DEV P8Ø S
DNP8Ø:     DN P8Ø
DNP8ØA:    DN P8Ø ALL
```

At Half Slot

```
UPDPØ8:    UP DEV PØ8
UPDPØ8S:   UP DEV PØ8 S
UPPØ8:     UP PØ8
UPPØ8A:    UP PØ8 ALL
DNDPØ8:    DN DEV PØ8
DNDPØ8S:   DN DEV PØ8 S
DNPØ8:     DN PØ8
DNPØ8A:    DN PØ8 ALL
```

■ Suffix code None

■ Initial setting UPDV (When system is PACS / PHS), UPDPØØ (When system is WCPE)

■ Example PAT␣UPT

PAT Pattern

■ Function Sets the internal modulation data pattern when the burst function turns off.

Header	Program command	Query	Response
PAT	PAT␣a	PAT?	PAT␣a

■ Value of a

PACS / PHS
ØØØØ to 1111 (optional 4 bits), PN9 , PN15

WCPE system
$ØØØØ_H$ to $FFFF_H$ (optional 4 bits), PN9 , PN15

■ Suffix code None

■ Initial setting PN9

■ Example PAT␣PN15

PAT Pattern in "Memory"

■ Function

Chooses the burst internal modulation data from 100 patterns in the burst pattern memory.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
PAT	PAT␣MEMa	PAT?	PAT␣MEMa

■ Value of a ØØ to 99

■ Suffix code None

■ Example PAT␣MEM3

PCC Power Control Channel

■ Function

Sets the PPC data of the downlink communications channel in the PACS system.
(When the burst function unit is supported, this function is available.)

Header	Program command	Query	Response
PCC	PCC␣a	PCC?	PCC␣a

■ Value of a #HØ to #H1 (Hexadecimal number)

■ Suffix code None

■ Initial setting #HØ

■ Example PCC␣#H1

P

PN Pseudo random

■ Function Sets the PN data of DEVICE slot.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
PN	PN␣a	PN?	PN␣a

■ Value of a PN9, PN15
■ Suffix code None
■ Initial setting PN9
■ Example PN␣PN15

PSID PS Identification Code

■ Function Sets the PS-ID data of SYNC slot in the PHS system.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
PSID	PSID␣a	PSID?	PSID␣a

■ Value of a #H0000000 to #HFFFFFFF (Hexadecimal number)
■ Suffix code None
■ Initial setting #H0000001
■ Example PSID␣#H0000003

R Reserved

■ Function

Sets the R data of the uplink communications channel in the PACS system. (When the burst function unit is supported, this function is available.)

Header	Program command	Query	Response
R	R␣a	R?	R␣a

■ Value of a #HØ to #H1 (Hexadecimal number)

■ Suffix code None

■ Initial setting #HØ

■ Example R␣#H1

S Sync Word

■ Function

Sets S data for the slot in the WCPE system.
(When the burst function unit is supported,this function is available)

Header	Program command	Query	Response
S	S␣a	S?	S␣a

■ Value of a #H00000000 to #HFFFFFFFF

■ Suffix code None

■ Initial setting #HAAAAE98A$_H$: Down link
#H55551675$_H$: Up link

■ Example S␣#HAAAAE98A

SA SACCH Slow Associated Control Channel

■ Function

Sets the SA data of VOX/TCH slot in the PHS system.
(When the burst function unit is supported,this function is available)

Header	Program command	Query	Response
SA	SA␣a	SA?	SA␣a

■ Value of a #H0000 to #HFFFF (Hexadecimal number)

■ Suffix code None

■ Initial setting #H8000

■ Example SA␣#HFFFF

SAD Symbol Adjust

■ Function Changes the synchronous state of symbol clock.

Header	Program command	Query	Response
SAD	SAD	———	———

■ Suffix code None

■ Example SAD

SC Slow Channel

■ Function Sets the SC data of the uplink/downlink communications channels in the PACS system.
(When the burst function unit is supported, this function is available.)

Header	Program command	Query	Response
SC	SC␣a	SC?	SC␣a

■ Value of a #HØØØ to #H3FF (Hexadecimal number)

■ Suffix code None

■ Initial setting #HØØØ

■ Example SC␣#H2E5

SCBL Scramble On/Off, CS-ID Scramble On/Off

■ Function

Sets On/Off for the CS-ID scramble function of the VOX/TCH slot and the scramble function of the SYNC slot of the PHS system.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
SCBL	SCBL␣a	SCBL?	SCBL␣a

■ Value of a

ON: On
OFF: Off

■ Suffix code

None

■ Initial setting

ON

■ Example

SCBL␣OFF

SCBLC Scramble Code, CS-ID Scramble Code

■ Function

Sets On/Off for the CS-ID scramble function of the VOX/TCH slot and the scramble function of the SYNC slot of the PHS system.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
SCBLC	SCBLC␣a	SCBLC?	SCBLC␣a

■ Value of a

PHS system: #HØØØ to #H3FF (Hexadecimal number)

■ Suffix code

None

■ Initial setting

PHS system: #H2ØØ

■ Example

PHS system: SCBLC␣#H3FF

SCRT Secret Scramble On/Off

■ Function

Turns on or off the Secret (Encryption) scramble function of VOX/TCH slot in the PHP.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
SCRT	SCRT␣a	SCRT?	SCRT␣a

■ Value of a

ON: On
OFF: Off

■ Suffix code

None

■ Initial setting

ON

■ Example

SCRT␣OFF

SCRTC Secret Scramble Code

■ Function

Sets the Secret Scramble (Encryption Key) code VOX/TCH slot in the PHS system.
(When the burst function unit is supported,this function is available)

Header	Program command	Query	Response
SCRTC	SCRTC␣a	SCRTC?	SCRTC␣a

■ Value of a

#H0000 to #HFFFF (Hexadecimal number)

■ Suffix code

None

■ Initial setting

#H0000

■ Example

SCRTC␣#HFFFF

SLOT Slot

■ Function

Modfies the slot contents of the internal modulation data.
(When the burst function unit is supported,this function is available)

Header	Program command	Query	Response
SLOT	SLOT␣a	SLOT?	SLOT␣a

■ Value of a

PACS

DEVICE
- On — SLOT␣UPDV
- Off — SLOT␣OFF

UP TCH
- UP TCH — SLOT␣UPT
- Off — SLOT␣OFF

UP TCH ALL
- UP TCH — SLOT␣UPT
- Off — SLOT␣OFF

DOWN TCH
- DOWN TCH — SLOT␣DNT
- Off — SLOT␣OFF

DOWN TCH ALL
- DOWN TCH — SLOT␣DNT
- Off — SLOT␣OFF

PHS

UP DEVICE
- On — SLOT␣ON
- Off — SLOT␣OFF

DOWN DEVICE
- On — SLOT␣ON
- Off — SLOT␣OFF

UP TCH:
- On — SLOT␣ON
- Off — SLOT␣OFF

UP TCH ALL:
- On — SLOT␣ON
- Off — SLOT␣OFF

DOWN TCH:
- DOWN TCH — SLOT␣DNT
- VOX — SLOT␣VOX
- Off — SLOT␣OFF

■ Value of a (cont.)

DOWN TCH ALL:
  DOWN TCH SLOT␣DNT
  VOX SLOT␣VOX
  Off SLOT␣OFF
UP VOX:
  On SLOT␣ON
  Off SLOT␣OFF
DOWN VOX:
  DOWN TCH SLOT␣DNT
  VOX SLOT␣VOX
  Off SLOT␣OFF
UP SYNC:
  UP TCH SLOT␣UPT
  UP SYNC SLOT␣UPSYNC
  Off SLOT␣OFF
DOWN SYNC:
  DOWN TCH SLOT␣DNT
  DOWN SYNC SLOT␣DNSYNC
  VOX SLOT␣VOX
  Off SLOT␣OFF

WCPE ——————————

At Full Slot

```
DPØØ:   DEV PØØ
DP32:   DEV P32
DPØØS:  DEV PØØ S
DP32S:  DEV P32 S
PØØ:    PØØ
P32:    P32
OFF:    Off
```

At Double Slot

```
DP8Ø:   DEV P8Ø
DP8ØS:  DEV P8Ø S
P8Ø:    P8Ø
OFF:    Off
```

At Half Slot

```
DPØ8:   DEV PØ8
DPØ8S:  DEV PØ8 S
PØ8:    PØ8
OFF:    Off
```

■ Suffix code None

■ Example SLOT␣OFF

SLOTNO Slot Number

■ Function

Selects the slot number in the pattern.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
SLOTNO	SLOTNO␣a	SLOTNO?	SLOTNO␣a

■ Value of a

The slot number range depends on the system.

For PACS system: Ø to 7
For PHS system: 1 to 4
For WCPE system: Full Slot Ø to 23
Double Slot Ø to 22 However, only even number.
Half Slot Ø, Ø to 23, 1
(If "a" is assumed to be "n" and "m", n is between 0 and 23, and m is between 0 and 1.)

■ Suffix code None

■ Initial setting 1 for the PHS system, and 0 for other systems

■ Example SLOTNO␣1

SYC Synchronization Bits

■ Function

Sets the SYC data of the downlink communications channel in the PACS system.
(When the burst function unit is supported, this function is available.)

Header	Program command	Query	Response
SYC	SYC␣a	SYC?	SYC␣a

■ Value of a #HØØØØ to #H3FFF (Hexadecimal number)

■ Suffix code None

■ Initial setting #HØØØØ

■ Example SYC␣#H12BA

PCC : Power control channel $Ø_H$ (1 bit)

SYS System

■ Function Selects the communication systems.

Header	Program command	Query	Response
SYS	SYS␣a	SYS?	SYS␣a

■ Value of a PACS, PHS, WCPE

■ Suffix code None

■ Initial setting PACS

■ Example SYS␣PHS

TC

■ Function — Sets the TC data of the slot in the WCPE system.
(When the burst function unit is supported,this function is available).

Header	Program command	Query	Response
TC	TC␣a	TC?	TC␣a

■ Value of a

For PØØ slot
PN9, PN15, #HØØØØØØØØ ~ #HFFFFFFFF

For P32, P8Ø, PØ8 slot
#HØØØØØØØØ ~ #HFFFFFFFF

■ Suffix code — None

■ Initial setting

For PØØ slot
PN9

For P32, P8Ø, or PØ8 slot
#HØFØFØFØF

■ Example — TC␣#HØØØØFFFF

TCH — Traffic Channel

■ Function — Sets the TCH data of TCH slot in the PHS system.
(When the burst function unit is supported,this function is available)

Header	Program command	Query	Response
TCH	TCH␣a	TCH?	TCH␣a

■ Value of a — PN9, PN15

■ Suffix code — None

■ Initial setting — PN9

■ Example — TCH␣PN15

TGS Burst Trigger Select

■ Function Selects the timing of the burst trigger in the PHS sytem.
(When the burst function unit is supported,this function is available)

Header	Program command	Query	Response
TGS	TGS␣a	TGS?	TGS␣a

■ Value of a UP: Uplink
DN: Downlink

■ Suffix code None

■ Initial setting DN

■ Example TGS␣DN

TQ

■ Function Sets the TQ data of the slot in the WCPE system.
(When the burst function unit is supported,this function is available)

Header	Program command	Query	Response
TQ	TQ␣a	TQ?	TQ␣a

■ Value of a #H00 to #HFF

■ Suffix code None

■ Initial setting #H21

■ Example TQ␣#H27

UW Unique Word

■ Function

Sets the UW data of VOX/TCH/SYNC slot in the PHS sytem.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
UW	UW␣a	UW?	UW␣a

■ Value of a

VOX/TCH slot: #H0000 to #HFFFF (Hexadecimal number)
SYNC slot: #H00000000 to #HFFFFFFFF (Hexadecimal number)

■ Suffix code

None

■ Initial setting

VOX/TCH slot: Uplink: #HE149
Downlink: #H3D4C
SYNC slot: Uplink: #H6B899AF0
Downlink: #H50EF2993

■ Example

UW␣#HFFFF

VOX Voice Operated Transmission

■ Function Sets the VOX data of VOX slot in the PHS system.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
VOX	VOX␣a	VOX?	VOX␣a

■ Value of a PN9, PN15

■ Suffix code None

■ Initial setting PN9

■ Example VOX␣PN15

Z　　Z Field

■ Function　　Sets the Z On/Off of the slot in the WCPE system.
(When the burst function unit is supported, this function is available)

Header	Program command	Query	Response
Z	Z␣a	Z?	Z␣a

■ Value of a　　ON, OFF
■ Suffix code　　None
■ Initial setting　　ON
■ Example　　Z␣OFF

4. SAMPLE PROGRAMS

This section describes some sample programs with the common commands and the program commands, queries, and response messages specific to the MG0307A

4.1 Generating π/4DQPSK Modulation Signal

< Example 1 > Sets the frequency to 1.5 GHz, output level to 0 dBm and communication system to NADC.

```
10  '------------------------------
20  ' MG3670B GPIB SAMPLE PROGRAM
30  ' OUTPUT π/4 DQPSK MODULATION
40  '------------------------------
50  ISET IFC ..... Initializes the interface function
60  ISET REN ..... Sets remote enable to TRUE
70  CMD DELIM=0 ..... Selects CR + LF as the delimiter
80  LET DSG=1 ..... Assigns MG3670 series address to variable DSG
90  PRINT @DSG;"PRE" ..... Initializes MG3670 series
100 SRQ ON ..... Permits the receipt of SRQ
110 PRINT @DSG;"*CLS" ..... Clears Status Byte Register
120 PRINT @DSG;"*SRE 4" ..... Masks bits other than SRE bit 2
130 PRINT @DSG;"ESE2 4" ..... Masks bits other than ESE2 bit 2
140 PRINT @DSG;"MOD ON" ..... Turns modulation on
150 PRINT @DSG;"MODE INT" ..... Sets the I,Q signals source to internal input
160 PRINT @DSG;"SYS PHS" ..... Sets the communication system to PHS
170 PRINT @DSG;"BST ON" ..... Turns the burst function on
180 PRINT @DSG;"PAT UPT" ..... Sets the standard internal modulation data to UP TCH
190 PRINT @DSG;"FREQ 1.5GHZ" ..... Sets the frequency to 1.5 GHz
200 PRINT @DSG;"OLVL 0DBM" ..... Sets the output Level to 0 dBm
210 POLL DSG,N ..... Performs serial polling
220 IF N<>68 THEN GOTO 210 ..... Exit from loop when STB ESB (bit 2) is 1
230 END
```

Lines 140 and 150 turn the modulation on and sets the I,Q signals source to internal input.
Lines 160 to 180 set the communication system to PHS, turns the burst function on,and sets the standard internal modulation data to Uplink traffic channel.
Lines 190 and 200 set the frequency and output level.
Lines 210 and 220 check that setting parameter has completed.

4.2 Setting the Internal Modulation Data

<Example 2> Sets the internal modulation data in the PHS system.

```
10  '------------------------------
20  ' MG3670B GPIB SAMPLE PROGRAM
30  ' PATTERN EDIT (PDC)
40  '------------------------------
50  ISET IFC
60  ISET REN
70  CMD DELIM=0
80  LET DSG=1
90  PRINT @DSG;"PRE"
140 PRINT @DSG;"MOD ON"
150 PRINT @DSG;"MODE INT"
160 PRINT @DSG;"SYS PHS"  ..... Sets the communication system to PHS
170 PRINT @DSG;"BST ON"   ..... Turns the burst function on
180 PRINT @DSG;"PAT UPT"  ..... Sets the standard internal modulation data to UP TCH
190 PRINT @DSG;"SLOTNO 2" ..... Sets the slot number to 2
200 PRINT @DSG;"SLOT UPT" ..... Sets the slot 2 to UP TCH
210 PRINT @DSG;"TCH PN15" ..... Sets the TCH data of slot 2 to PN15
220 PRINT @DSG;"SA #H12AB" .... Sets the SA data of slot 2 to 12AB (Hexadecimal number)
230 END
```

Lines 160 to 180 set the communication system to PHS, turns burst function on, and sets the standard internal modulation data to UP TCH.

Line 190 sets the slot number to 1.
Line 200 sets the slot 2 to UPTCH.
Lines 210 and 220 set the TCH data of slot 2 to PN15, and the SA data of slot 1 to 12AB (Hexadecimal number).

www.manualsplus.com
1030552